PROPOSAL FOR EXPERIMENT AT RCNP

January 19, 2012

TITLE:
SER Measurement on a 65nm LSI

SPOKESPERSON:

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EXPERIMENTAL GROUP:

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Jun Furuta	Graduate School of Informatics, Kyoto University	Graduate Student(M1)
Chikara Hamanaka	Graduate School of Science and Technology, Kyoto Institute of Technology	Graduate Student(M1)

RUNNING TIME: Installation time without beam .5 days(for each beam time)
Test running time for experiment .5 days
Data runs 2 days

BEAM LINE: RING Cyclotron : WN course

BEAM REQUIREMENTS:
Type of particle proton
Beam energy 392 MeV
Beam intensity $\leq 1\mu$A

BUDGET: Experimental expenses 0 yen

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SUMMARY OF THE PROPOSAL

Soft errors on LSIs are categorized to SEU (Single Event Upset) and SET (Single Event Transient). Workstations for high reliability contains SRAMs with ECC but also FFs with some error resiliency for SEU. But due to the higher clock rates on current high-end processors soft errors caused by SETs are increasing. To prevent soft errors from SET pulses, delay elements such as inverters or buffers are generally used. We have to investigate SET pulse width distributions to design most area-efficient but effective delay elements for SETs. We are going to measure SET pulse width distributions to compute SERs from SETs.

C-element prevents SEUs to latch the previous captured values if one of master/slave latches are flipped. SET pulses are removed by delay elements. But its vulnerability is just ten times bigger than the ordinal non-redundant FF since C-element is weak for SETs. We propose a modified circuit structure.We are going to measure the error rate of the conventional and proposed dual-modular FFs.

Multiple SRAM cells are flipped by a single particle hit, which is called MCU (Multiple Cell Upsets). MCU is caused by turning on parasitic bipolar transistors on the CMOS structure. If well-taps are sparsely laid out, the well voltage are elevated by a particle hit and then the bipolar transistors are turned on. We are going to design several circuit blocks with different well-tap structures to measure dependence of the well-tap density to SERs.

We will measure these three types of circuit structures on an LSI which will be fabricated in a 65nm process.