E385

RCNP EXPERIMENT

PROPOSAL FOR EXPERIMENT AT RCNP

TITLE:

Neutron-induced Soft Error Characterization and Experimental Validation of Radiation Hardened Circuits on 65nm bulk/SOI VLSIs

SPOKESPERSON:

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EXPERIMENTAL GROUP:

Name	**Institution**	**Position**
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K. Kobayashi	Graduate School of Sci. & Tech., Kyoto Institute of Tech.	Professor
J. Furuta	Graduate School of Informatics, Kyoto University	Student (D1)
R. Harada	Graduate School of Info. Sci. & Tech., Osaka Univ.	Student (D1)
H. Konoura	Graduate School of Info. Sci. & Tech., Osaka Univ.	Student (D1)

RUNNING TIME:	Installation time without beam	.5 days (for each beam time)
	Test running time for experiment	.5 days
	Data runs	3 day
BEAM LINE:	RING Cyclotron, WN course	
BEAM REQUIREMENTS:	Type of particle	proton
	Beam energy	392 MeV
	Beam intensity	1 μA
BUDGET:	0 yen	
NOTE:		

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Neutron-induced Soft Error Characterization and Experimental Validation of Radiation Hardened Circuits on 65nm bulk/SOI LSIs

SPOKESPAERSON: Masanori Hashimoto

SUMMARY OF THE PROPOSAL

Along with the scaling of semiconductor devices, single event multiple faults, which is a kind of soft error that two or more nodes are affected by one radiation particle, is becoming a serious problem. Single event multiple faults is mainly classified into single event multiple(-bit) upsets (SEMU), which causes bit flips in two or more memory elements, and single event multiple transients (SEMT), which induces pulses in two or more combinational logic nodes. For SEMT, we have devised a measurement circuit and presented the first measurement result [Harada, IRPS2011]. However, the measurable spatial distribution was limited in the test chip. In this measurement [**M1**], SEMTs widely spread on a 65nm bulk LSI are characterized with a newly designed test chip.

Recently, SOI (Silicon on Insulator) structure instead of conventional bulk structure is drawing attention for low power LSI (Large Scale Integration) implementations and a national project called LEAP (Low power Electronics Association & Project) is developing a dopant-less fully-depleted SOI transistor. This transistor is expected to have a better immunity to radiation because the sensitive volume to directly cause a soft error is limited to very thin buried oxide (BOX) layer compared to conventional bulk structure (See Figure 1). In addition, bipolar action due to a parasitic bipolar transistor is not thought to be activated. On the other hand, the BOX region is coupled with Si-Substrate through a capacitance originating from SiO_2-Insulator. This means that back-gates of SOI transistors could be affected by radiation through the capacitance and a particle may cause multiple faults. However, there are no measurement results to clarify if this capacitive coupling could cause soft errors. In this experiment [**M2**], we will design the same SEMT measurement circuit and characterize SEST (single event single transient) and SEMT on a SOI LSI in addition a bulk LSI for a comparative study.

We have proposed a dual-modular FF called Cross-coupled Dual Modular Redundancy Flip-Flop (BCDMR-FF, Figure 2) [Furuta, VLSI Circuits 2010], and confirmed the fundamental immunity to neutron. Besides, the overall immunity is dependent not only circuit structure but also layout. This experiment [**M3**] will evaluate the immunity of BCDMR-FF with improved layout. In addition, the same BCDMR-FF is fabricated in a 65nm SOI process and the immunity is compared with that of bulk process.

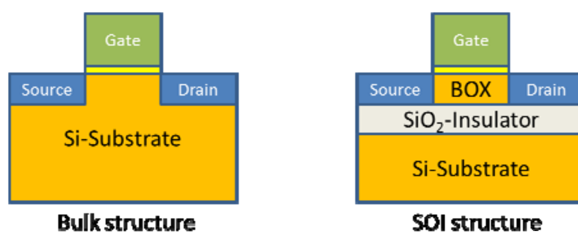

Figure 1: Bulk and SOI structures.

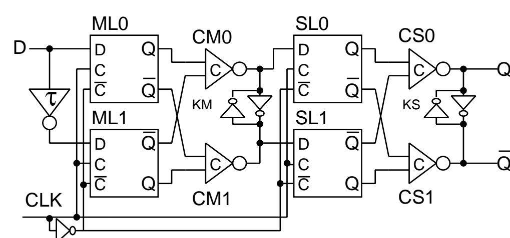

Figure2: BCDMR FF.