

**E410**

**PROPOSAL FOR EXPERIMENT AT RCNP**

July 17, 2012

**TITLE:****Ultra Low-power Circuits for Future Highly-reliable Embedded Systems.****SPOKESPERSON:**

Full Name	Kazutoshi Kobayashi
Institution	Department of Electronics, Graduate School of Science and Technology, Kyoto Institute of Technology
Title or Position	Professor
Address	Matsugasaki, Sakyo, Kyoto, 606-8585
Phone number	+81-75-724-7452
FAX number	+81-75-724-7452
E-mail	kazutoshi.kobayashi@kit.ac.jp

**EXPERIMENTAL GROUP:**

K. Kobayashi	Graduate School of Sci. & Tech., Kyoto Inst. of Tech.	Professor
Y. Watanabe	Graduate School of Eng. Sci, Kyushu Univ.	Professor
M. Hashimoto	Graduate School of Info. Sci. & Tech., Osaka Univ.	Associate Professor
J. Furuta	Graduate School of Informatics, Kyoto University	Ph.D. Candidate (D2)
R. Harada	Graduate School of Info. Sci. & Tech., Osaka Univ.	Ph.D. Candidate (D2)
S. Abe	Graduate School of Eng. Sci, Kyushu Univ.	Ph.D. Candidate (D3)

**RUNNING TIME:** Installation time without beam .5 days(for each beam time)  
 Test running time for experiment .5 days  
 Data runs 4 days

**BEAM LINE:** RING Cyclotron : WN course

**BEAM REQUIREMENTS:** Type of particle proton  
 Beam energy 392 MeV  
 Beam intensity  $\leq 1\mu\text{A}$

**BUDGET:** Experimental expenses 0 yen

**TITLE:**

**Ultra Low-power Circuits for Future Highly-reliable Embedded**

**SPOKESPERSON:** Kazutoshi Kobayashi

**SUMMARY OF THE PROPOSAL**

We are developing ultra low-power circuits for future highly-reliable embedded systems that operate with dry batteries as long as possible, or rather without battery by scavenging environmental energy. Our experiments expose 65-nm SOTB (Silicon on Thin BOX) chips at very-low-voltage power supply such as 0.1 V or 0.4 V. The goals of this experiment are 1) investigating the fundamental immunity of SOTB device since its immunity has been neither measured nor reported, and 2) validating existing techniques developed for bulk CMOS and SOI.