E434

RCNP EXPERIMENT E

PROPOSAL FOR EXPERIMENT AT RCNP

February 11, 2014

TITLE:
Low-power Highly-reliable Integrated Circuits.

SPOKESPERSON:

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EXPERIMENTAL GROUP:

K. Kobayashi	Graduate School of Sci. & Tech., Kyoto Inst. of Tech.	Professor
Y. Watanabe	Graduate School of Eng. Sci, Kyushu Univ.	Professor
M. Hashimoto	Graduate School of Info. Sci. & Tech., Osaka Univ.	Associate Professor
S. Abe	Graduate School of Eng. Sci, Kyushu Univ.	Researcher

RUNNING TIME: Installation time without beam — .5 days(for each beam time)
Test running time for experiment — .5 days
Data runs — 4 days

BEAM LINE: RING Cyclotron : WN course

BEAM REQUIREMENTS:
Type of particle — proton
Beam energy — 392 MeV
Beam intensity — $\leq 1\mu$A

BUDGET: Experimental expenses — 0 yen

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SUMMARY OF THE PROPOSAL

We are developing ultra low-power circuits for future highly-reliable systems that operate with dry batteries as long as possible, or rather without battery by scavenging environmental energy. Our experiments expose 65-nm SOTB (Silicon on Thin BOX) and 28-nm UTBB (Ultra-thin Body and BOX) semiconductor chips at very-low-voltage power supply such as 0.6 V. The goals of this experiment are 1) investigating the fundamental immunity of SOTB and UTBB devices, and 2) validating existing techniques developed for bulk CMOS and SOI (Silicon on Insulator).