

PROPOSAL FOR EXPERIMENT AT RCNP

Feb. 14th, 2016

TITLE:**Low-power Highly-reliable Integrated Circuits.****SPOKESPERSON:**

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EXPERIMENTAL GROUP:

K. Kobayashi	Graduate School of Sci. & Tech., Kyoto Inst. of Tech.	Professor
Y. Watanabe	Graduate School of Eng. Sci, Kyushu Univ.	Professor
J. Furuta	Graduate School of Sci. & Tech., Kyoto Inst. of Tech.	Assistant Professor

RUNNING TIME: Installation time without beam .5 days(for each beam time)
 Test running time for experiment .5 days
 Data runs 2 days (48 hours)

BEAM LINE: RING Cyclotron : WN course

BEAM REQUIREMENTS: Type of particle proton
 Beam energy 392 MeV
 Beam intensity $\leq 1\mu\text{A}$

BUDGET: Experimental expenses 0 yen

TITLE:

Low-power Highly-reliable Integrated Circuits.

SPOKESPERSON: Kazutoshi Kobayashi

SUMMARY OF THE PROPOSAL

We are developing ultra low-power circuits for future highly-reliable systems that operate with dry batteries as long as possible, or rather without battery by scavenging environmental energy. Our experiments irradiate 65-nm SOTB (Silicon on Thin BOX), 28-nm UTBB (Ultra-thin Body and BOX) and 16-nm FinFET semiconductor chips at very-low-voltage power supply such as 0.6 V. The goals of this experiment are 1) investigating the fundamental immunity of SOTB and UTBB devices, and 2) validating existing techniques developed for bulk CMOS and SOI (Silicon on Insulator), and 3) clarifying the correlation between hardware and simulation.