Flash Analog-Digital-Converter Module for Time Projection Chamber at SPring-8/LEPS

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One of the upgrade projects of LEPS/SPring-8 experiment in year 2002 is the construction of Time Projection Chamber (TPC) [1]. Complementary to the extreme forward acceptance of the existing spectrometers, TPC provides a wide acceptance in the backward direction, where *e.g.* kaons from the low-momentum ϕ mesons decaying inside nuclei target can be measured for study of nuclear medium effect. It is also designed with the capability of detection of decay topology in high resolution which is essential for distinguishing $\Lambda^*(1405)$ from $\Sigma^*(1385)$. The 3-dimensional trajectory of charged particle is determined by the energy loss in the effective volume of TPC as a function of sampling time. The maximum drifting time is about 15 μsec corresponding to the active drifting length of 70 cm and drift velocity of 5.2 cm/μsec. There are a total of 1055 cathode pads for read-out.

In order to achieve the required spatial resolution (300 μm in x,y and 700 μm in z) and large dynamic range of particle identification using energy loss, we design Flash Analog Digital Converter (FADC) system for digitization of analog signals from pre-amplifiers, based on the following requirement:(1) a resolution of 10-bit at 40 MHz sampling rate (2) event buffer large to hold 4-5 events for one cycle of VME/READ (3) on-board zero suppression to save DAQ load (4) high channel density.

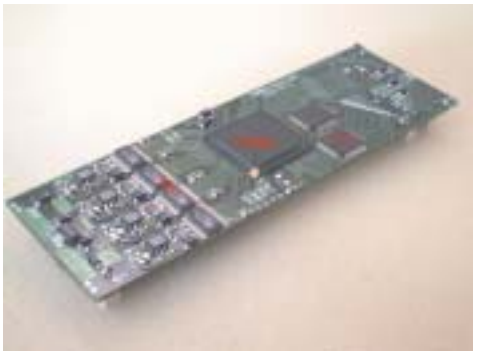

Figure 1: Photo of 4-channel FADC daughter card.

Mechanical size	Eurocard 9U, single width
Number of channels	32
Analog input	0 to +2.0 V
Input impedance	50 Ω for twisted pair cable
Gain	x 1
Input offset	400 mV (variable)
Dynamic range	10-bit
Sampling rate	40 MHz with external CLOCK
Data FIFO	16 bits x 4096 per channel
Inputs: NIM level	TRIGGER, RESET, CLOCK
Outputs: NIM level	BUSY

Table 1: Specifications of the LEPS-FADC board

The LEPS-FADC board is composed of a VME-9U mother board and 8 pieces of detachable 4-channel FADC daughter cards [2]. The FADC daughter card shown in Fig. 1 consists of 4-channel analog circuits and AD9203 A/D converter chips. One Field Programmable Gate

Array (FPGA) of model Xilinx XC2S150 in each daughter performs the zero-suppression data reduction and event formatting. Digitized ADC data above suppression threshold in one clock cycle of 25 nsec are written into FIFO (TI SN74V245-20) with 4096 depth for each channel, large enough to hold 5-6 events with a reasonable estimate of signal occupancy.

On the VME-9U mother board, a chip of Complex Programmable Logic Device (CPLD), Xilinx XC95288XL-6, works as the interface between each FADC channel and VME bus. It receives external START trigger from the front panel input and issue out VME/IRQ when the triggered events reach the specified number (range:1-8). The control logic of FADC responding to the receipt of triggers is schemed in Fig. 2. Number of events for issuing VME/IRQ and the zero-suppression threshold value channel by channel can be configured by VME/WRITE. Details of the specification of FADC is listed in Table. 1.

We have fabricated 40 units of LEPS-FADC modules, equal to 1280 channels totally, in Taiwan in Dec, 2002. Properties of gain, linearity and zero-suppression were tested. Fig. 3 shows a nice agreement of a fitting curve with the measurement of an input pulse of 1 MHz sine wave. The LEPS-FADC modules were then shipped and installed in the LEPS/SPring-8 in March, 2003. In the recent cosmic ray test, LEPS-FADC system has been successfully exercised with the TPC detector and UNIDAQ DAQ system. The quality of gain and linearity of the complete system has been measured to be within the design specifications [3]. Commission run of TPC in LEPS experiment has been scheduled in June, 2003. We expect to start physics runs for the study of nuclear medium effect of ϕ mesons and properties of $\Lambda^*(1405)$ in the latter half year of 2003.

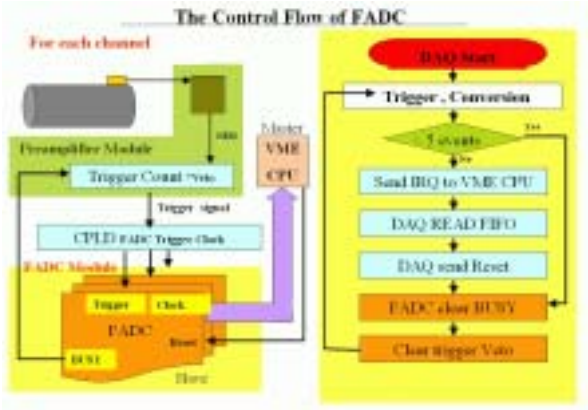

Figure 2: Control logic of FADC responding to the receipt of triggers

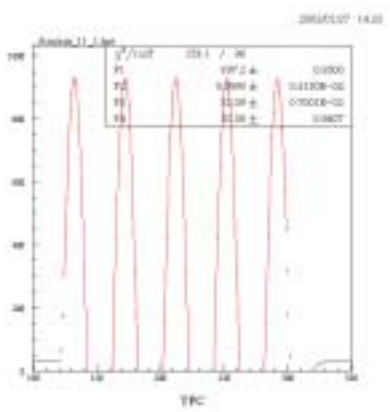

Figure 3: Fitting of FADC measurement of 1 MHz sine wave input.

References

[1] M. Niiyama *et al.*, RCNP Annual Report 2001, p.119.
[2] http://www.phys.sinica.edu.tw/~spring8/TPC_WWW/SPring-8-FADC-Manual.htm
[3] M. Niiyama *et al.*, RCNP Annual Report 2002.