

## Soft-error measurement of logic devices using quasi-monoenergetic neutron beam

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As the dimensions and operating voltage of semiconductor devices are reduced, neutron-induced soft error becomes an increasingly serious issue in logic devices [1-3]. The soft errors occur in not only embedded SRAMs but also in logic circuits such as the data-latch circuit. We investigated the neutron energy dependence of the single-event-upset (SEU) cross section in embedded SRAMs and flip-flop circuits by using the quasi-monoenergetic neutron beam, and demonstrated the characteristics of the logic device soft error.

We performed an irradiation test using the quasi-monoenergetic neutron beam at the Research Center for Nuclear Physics (RCNP) at Osaka University. The neutron beam was produced by the  ${}^7\text{Li}(p,n){}^7\text{Be}$  reaction. The energies of the neutron beam used in this experiment were 14, 26, 62, 98, 148 and 198 MeV. To clarify the effects of radiation on the logic device, we have used the embedded SRAMs (Type1, 2, etc.) with various cell sizes and a special test structure called FFRAM, which consists of a large number of flip-flop circuits accessed randomly. The FFRAM is equivalent to a 213Kbit (213K flip-flop circuits) RAM. These embedded SRAMs and FFRAMs were fabricated in 0.18 $\mu\text{m}$  (1.8V), 0.15 $\mu\text{m}$  (1.5V) and 0.13 $\mu\text{m}$  (1.2V) CMOS processes.

The SEU cross sections of 0.18 $\mu\text{m}$ /0.13 $\mu\text{m}$  embedded SRAMs and FFRAMs with the minimum cell size as a function of the neutron energy are shown in figs. 1 (a) and (b), respectively. It is well known that the SEU cross section increases rapidly with neutron energy and saturates in the high-neutron-energy region. The same tendency was observed in both 0.18 $\mu\text{m}$  and 0.13 $\mu\text{m}$  embedded SRAMs. The energy at which the SEU cross section was saturated shifts to the low-energy side as the design rule is scaled down.

The node charge dependence of SER per bit in the various embedded SRAMs and FFRAMs of the 0.18 $\mu\text{m}$ -0.13 $\mu\text{m}$  nodes is shown in fig. 2. The slope of the SER in relation to the node charge is different in each technology. However, although the technology is scaled down, the SERs for the same types of SRAMs and FFRAMs are almost constant or slightly decreased. Furthermore, it is found that the SER of the FFRAM is approximately 1/3~1/5 that of the embedded SRAM for all technology nodes. Taking into account the increasing number of logic circuits with technology downscaling, the SER of logic circuits can no longer be ignored.

We investigated the soft error of the 0.18 $\mu\text{m}$ -0.13 $\mu\text{m}$  embedded SRAMs and flip-flop circuits in logic devices using a quasi-monoenergetic neutron beam. As technology is scaled down, the SER of both embedded SRAM and flip-flop circuit remains almost constant or slightly decreases. Hence, the SER trend of chip level tends to increase in proportion to the circuit scale.

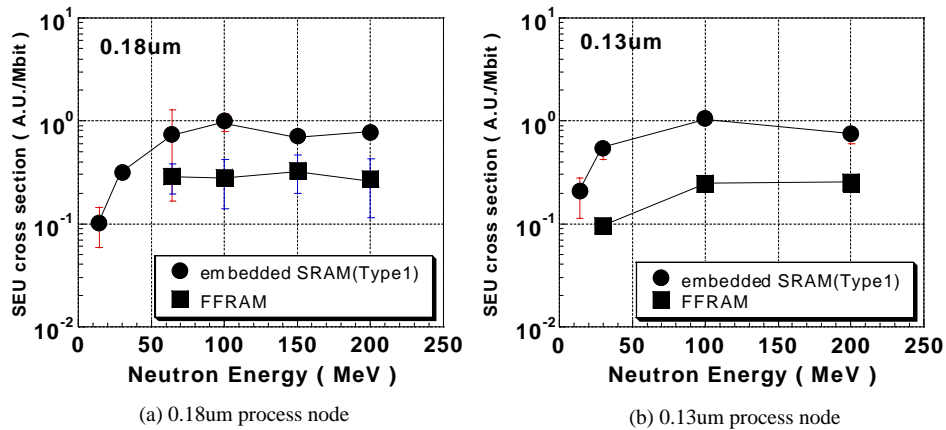


Fig. 1. SEU cross section in embedded SRAMs and FFRAMs as a function of neutron energy

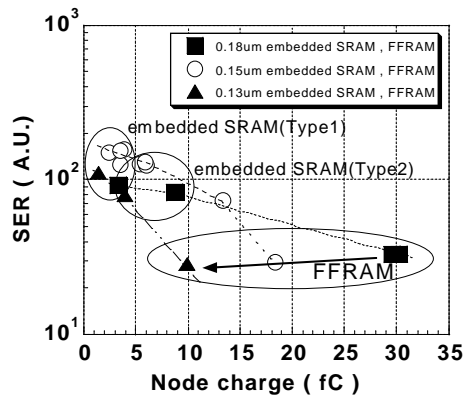


Fig. 2. SER in embedded SRAMs and FFRAMs of 0.18 $\mu\text{m}$ , 0.15 $\mu\text{m}$  and 0.13 $\mu\text{m}$  technology node as a

## References

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