Development of a FPGA-based high resolution TDC using Xilinx Spartan-6

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We have been developing a high resolution time to digital converter (TDC) using a field programmable gated array (FPGA). In future experiments such as J-PARC E50, low cost and short dead time TDC whose time resolution of better than 30 psec is needed. FPGA-based high resolution TDC (HR-TDC) is a strong candidate because it is now a feasible technology[**?**, **?**] to meet the requirement and successfully used in hadron and nuclear physics experiment[**?**].

We have studied the implementation of FPGA-based HR-TDC by using Xilinx Spartan-6 (XC6SLX150-2FGG484C) mounted on a KEK-VME-6U board (DRS4QDC)[**?**]. The TDC uses two types of counters; coarse counter and fine counter. Coarse counter measures time by clock-counting with a clock frequency of 375 MHz, which is the fastest frequency to drive the global clock in the target device. Fine counter interpolates the clock interval of 1/375 MHz (=2.67 nsec) by a tapped delay line, which consists of a carry chain and D-flipflop arrays. The carry chain contains fast multiplexers, which work as short delay elements, and D-flipflops capture a snapshot of the pulse propagation in the delay line. The front edge position of the pulse is encoded in a binary code, then, it is converted to time information. A typical delay amount of each tap (or a bin width) is a few tens psec. However, the bin width varies from bin to bin depending on the FPGA internal structure. To compensate the bin width variation, a look-up-table (LUT) is built by a statistical code density test, which uses a linear relationship between the bin width and the number of edge detection of the input signal on the corresponding bin. The LUT-building sequence runs automatically using a block RAM. First it accumulates the number of detected pulse edges like a histogram, then the bin contents are integrated. Finally the contents are normalized so that the block RAM stores the fine counter. For the precise calibration, a clock of 26.4528 MHz (= 375 MHz $\times 32/5/31$) is synthesized by cascading the PLLs in the FPGA[**?**] and used as a test input signal. The calibration pulse with the special frequency is captured at 4096 different phases to the sampling clock of 375 MHz, which is expected to be equally distributed with a step of 0.65 psec (=2.67/4096 nsec) in the sampling clock interval.

A typical LUT and bin width obtained by the above calibration are shown as black lines in Fig.**??** and Fig.**??**, respectively. About 145 taps are needed to interpolate the sampling clock interval. Mean bin width of $\sim$20 psec was obtained. The TDC performance was checked by NIM signal from a logic board. Figure **??**(a) shows a time difference of the hit input and a common stop. The time resolution of 28 psec (σ) was obtained. Assuming that the both channels have the same time resolution, the single channel resolution can be calculated by dividing the width by $\sqrt{2}$. It corresponds to 20 psec ($=28/\sqrt{2}$).

FPGA-based TDC has a flexibility in the implementation and room to improve its performance by multiple measurement of the same hit at the cost of the resource usage. Wave union TDC invented by Wu[**?**] is a resource effective implementation because the multiple measurements are performed in one delay line. We have tried applying a wave union technique to the Xilinx Spartan-6. In the current study, "wave union launcher A"[**?**], which generates a fixed pulse pattern having two pulse edges from one hit input, was implemented. The tap positions of the two edges of the wave union were encoded in binary code simultaneously and sum of them were used as virtual bin ID of LUT. Red lines in Fig.**??** and Fig.**??** indicates a typical LUT and virtual bin width of the wave union TDC, respectively. The number of taps is almost doubled and the bin widths are reduced to a half of those without wave union. The performance was checked using NIM signal in the same way. However, time resolution was not improved so much as shown in Fig.**??**(b) in spite of the fact that there was a potential for better resolution owing to the fine LUT. Although the reason has not yet been fully understood, one of the possibility is that signal integrity in front of FPGA input pin might cause the worse resolution.

After the demonstration of our wave union TDC implementation, a multi-hit buffer was added into the TDC, which is pipelined and runs with no deadtime. The current firmware of L1-buffer has $\sim$43 µsec time range with 256 hit depth per channel, which is shared by leading-edge and trailing-edge measurements. We

could implement 16×2+1 tapped delay lines with wave union launcher in the Spartan-6-150LX, where leading-edge and trailing-edge measurements of 16 input signals and a common stop measurement use 32 and one delay lines, respectively. The performance evaluation is ongoing.

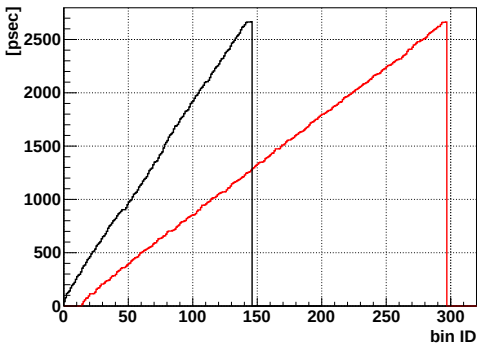


Figure 1: Calibration Look-up-Table of FPGA-based HR-TDC. black: without wave union. red: with wave union.

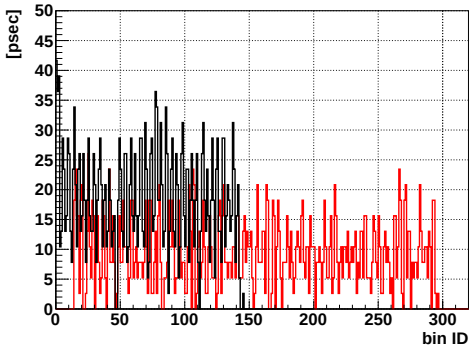
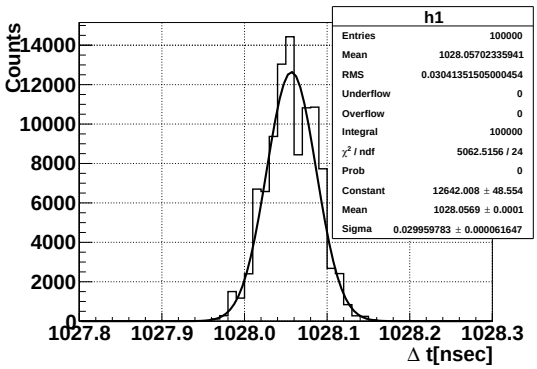
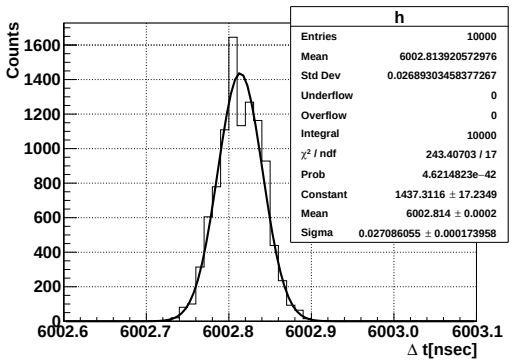


Figure 2: Bin width of the delay line. black: without wave union. red: with wave union.



(a) without wave union



(b) with wave union

Figure 3: Preliminary results of time difference between a hit and common stop. Single channel resolution (σ) is ∼20 psec($= 28/\sqrt{2}$) in the both cases of with/without wave union.

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