RCNP EXPERIMENT E347

PROPOSAL FOR EXPERIMENT AT RCNP

14 July 2009

TITLE:
Evaluation of SET pulse distribution and SEU immunity of subthreshold SRAM in 65nm integrated circuits

SPOKESPERSON:

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EXPERIMENTAL GROUP:

Name	Institution	Title or Position
M. Hashimoto	Graduate School of Info. Sci. & Tech., Osaka Univ.	Associate Professor
Y. Mitsuyama	Graduate School of Eng., Osaka Univ.	Assistant Professor
H. Fuketa	Graduate School of Info. Sci. & Tech., Osaka Univ.	Student (D2)
R. Harada	Graduate School of Info. Sci. & Tech., Osaka Univ.	Student (M1)

RUNNING TIME:

Setup and DAQ test	0.5 day
Data runs	1 day

BEAM LINE: WN course

BEAM REQUIREMENTS:

Type of particle	proton
Beam energy	392 MeV
Beam intensity	IμA

BUDGET: 0 yen

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SUMMARY OF THE PROPOSAL

Soft errors in VLSI consist of SEU (Single Event Upset) and SET (Single Error Transient).

Fault operations due to SET has been attracting attention recently, since SET pulses that arise in combinational circuits are more often captured into FFs as clock frequency increases. Estimating error probability due to SET and reducing errors need the distribution of SET pulse widths. In literatures, some measurement results have been reported, however they are not sufficient in the following points; the number of pulses is not large enough from a statistical point of view, and/or the time resolution of measurement circuits is not high enough. This proposed experiment aims to acquire an accurate distribution of SET pulses that occurs inside combinational circuits by using the measurement circuitry with high time resolution that we have developed.

Recently, a national project that aims at VLSI design for 0.5V operation has started with the initiative of the Ministry of Economy, Japan, and lowering supply voltage has been regaining wide attention. On the other hand, when the supply voltage is aggressively reduced, it is not clear how much immunity to soft errors VLSI has. At lower supply voltage, critical charge is generally small, and the immunity to soft errors deteriorates. Meanwhile, in subthreshold circuits whose supply voltage is near or below transistor threshold voltage, electrical field near drain is weak, and charge generated by coincidence of neutrons is no longer strongly drifted to drain. This experiment would experimentally clarify the SEU robustness of subthreshold SRAM.

We evaluate SET appearing in subthreshold combinational circuits. We are thinking that multiple SETs may arise due to a coincidence of a single neutron similar to multiple bit upsets in SRAM. SET rate of subthreshold combinational circuits would be evaluated varying supply voltage and body biasing.