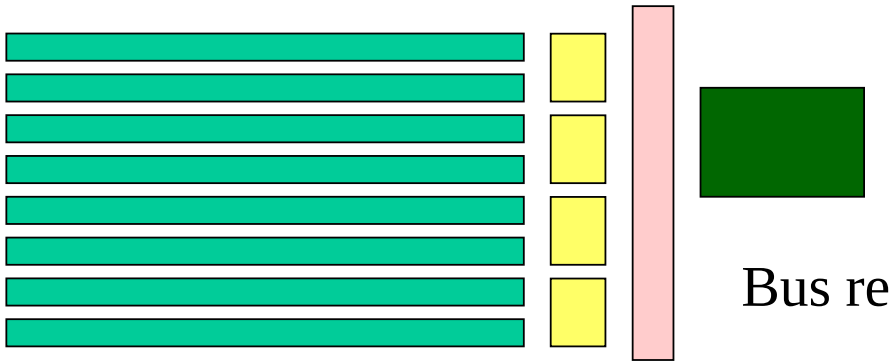
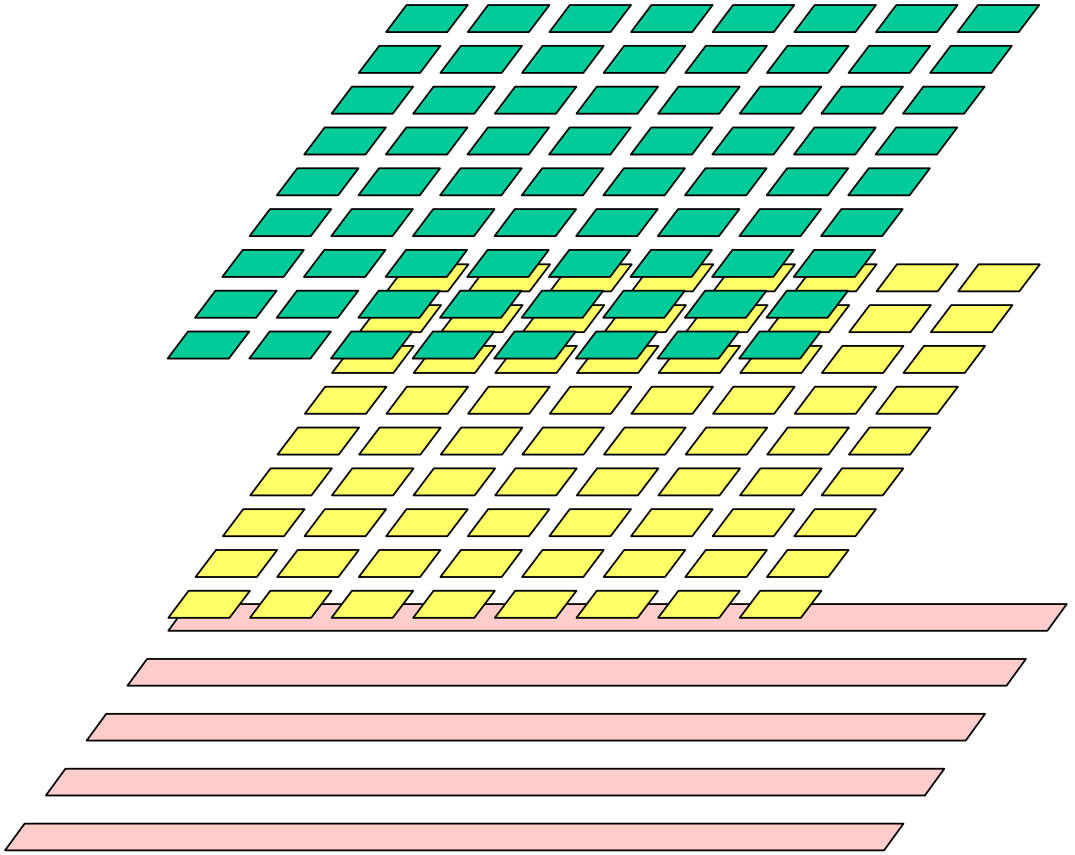
Data acquisition system on serial data link

M. Nomachi
Osaka University, Japan



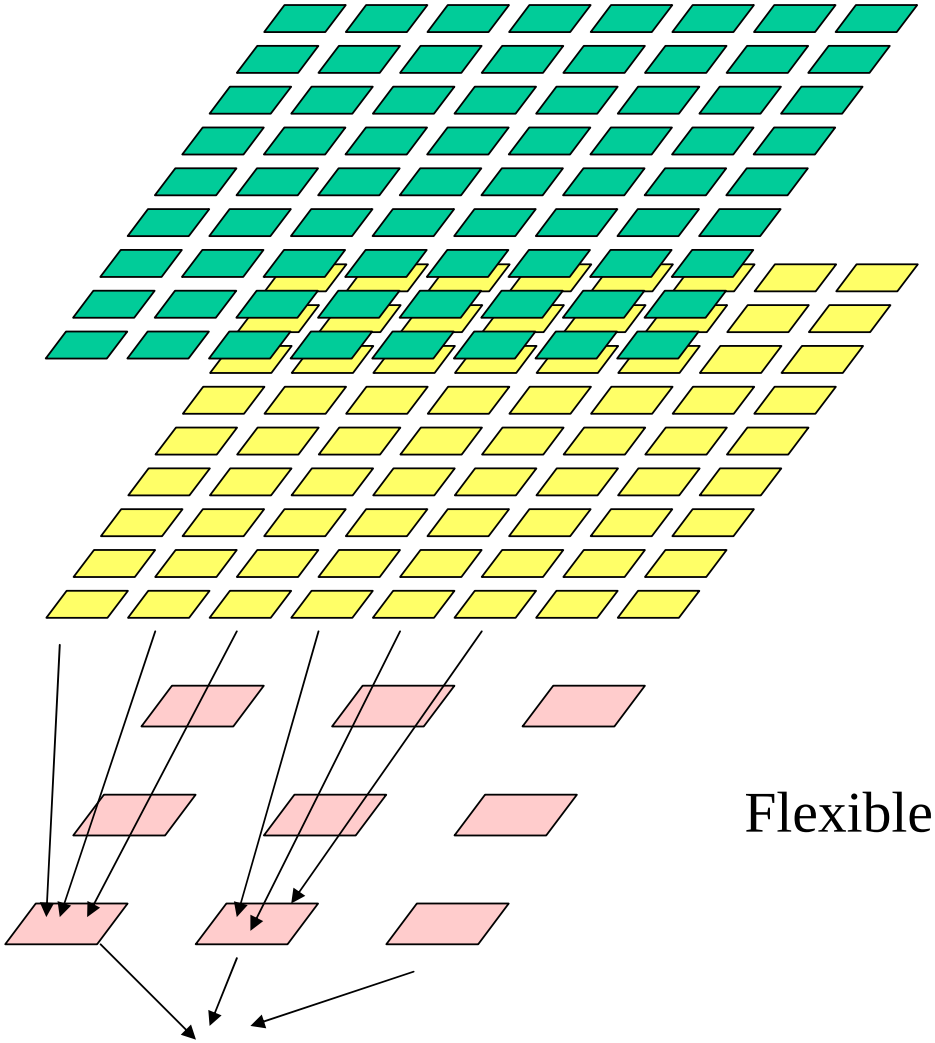
Bus readout



Bus readout

Space

Data processing on the fly



Flexible configuration

BUS vs. Serial link

BUS	Serial link
133MHz x 64 bit ~800MB/s VME single access ~8MB/s	300 Mbps ~30 MB/s Single access 2~3MB/s
64 line x 10mA(?) = 640mA	4 line x 3.5mA(LVDS) = 14mA
200~500ns latency BLT has longer latency	~1μs latency

Serial data transfer

フロントエンドで使用するためには

- フロントエンドの小規模なchipに実装できる簡単なプロトコル。

  多くのシリアル転送ではクロックの再構築のためのＰＬＬが必要であるが、フロントエンドで使用するにはＰＬＬがなくても動作するプロトコルが望ましい。

- 高速レスポンスを実現するための短い遅延時間。

  パイプライン処理を行わないフロントエンドでは遅延時間がそのままDead Timeとなってしまう。このため余計な処理を行わない単純なプロトコルが望ましい。

- ノイズ源とならない信号レベル。

  デジタル信号の遷移はアナログ系のノイズ源となる。このため、ＬＶＤＳ等、振幅の小さい信号レベルが望ましい。

Serial data link

	signal	speed	Code		Logic size	
PCIExpress	LVDS	2.5Gbps	8B/10B	Virtex-II Pro	8K~10K LE	PLL
SpaceWire	LVDS	400Mbps	SD link	Cyclone	~1K LE	No PLL
Infiniband	LVDS	2.5Gbps	8B/10B			
Switched Fabric	LVDS	622Mbps	8B/10B			

Standard for Space application
ESA standard

SpaceWire Key Features

- Serial, bi-directional, full duplex
- High data rate (> 200 Mbits/s)
- Distance of 10 m +
- Low gate count
- Can be implemented in FPGAs
- Scalable
- Low error rate
- Good EMC performance
- Fault tolerant support
- Radiation tolerant components

Steve Parkes 2005

SpaceWire

4Links™

	Modular One	Trans-puter	T9000	IEEE 1355	SMCS	Space-Wire
Point-to-point	✓	✓	✓	✓	✓	✓
Symmetrical	✓	✓	✓	X	X	✓
Asynchronous	✓	✓	✓	✓	✓	✓
Flow-controlled	✓	✓	✓	✓	✓	✓
Modular	✓	✓	✓	✓	✓	✓
Scalable	✓	✓	✓	✓	✓	✓
Fault-tolerant	✓	✓	✓	✓	✓	✓
Serial		✓	✓	✓	✓	✓
DMA engine		✓	✓		✓	?
Packet protocol			✓	✓	✓	✓
Virtual Channels			✓			?
Network protocol			✓			✓
Time distribution				(Fibre)		✓
Comms instructions		✓	✓			?

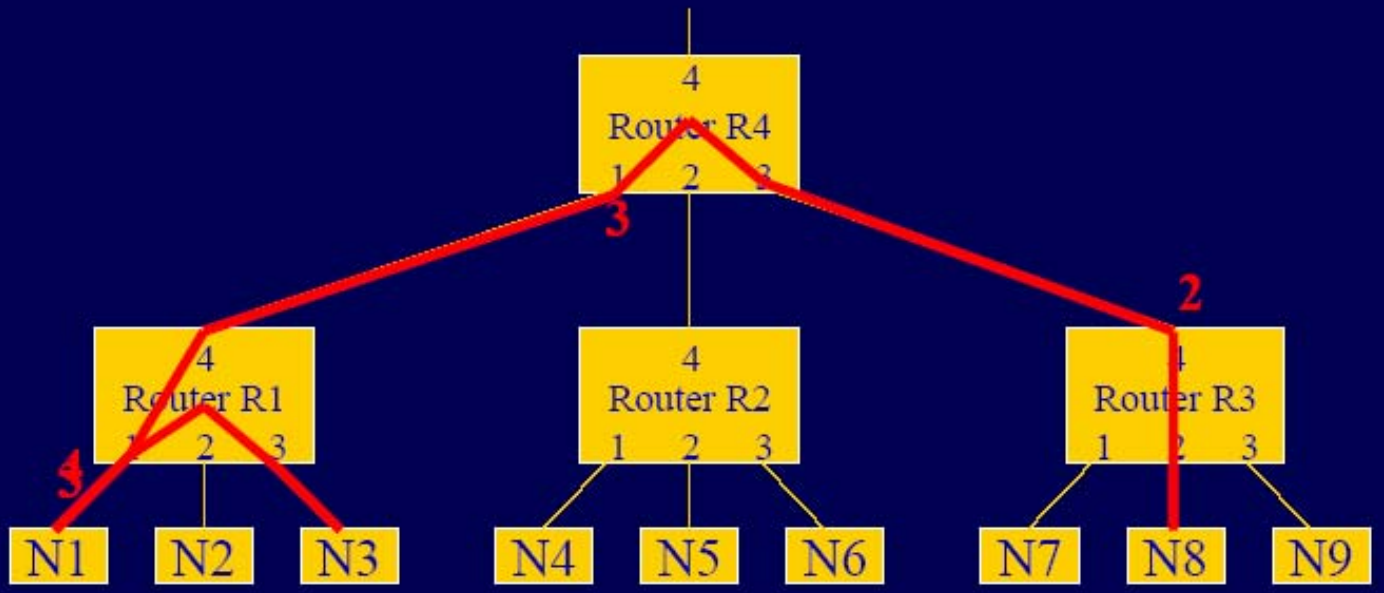
SpaceWire Packets

- Packet Format
- <DESTINATION> <CARGO> <END OF PACKET MARKER>
- Destination
  - represents either path to, or identity of destination node
- Cargo
  - data or message to be transferred from source to destination
- End of Packet Marker
  - indicates end of packet

Steve Parkes 2003

Path Addressing

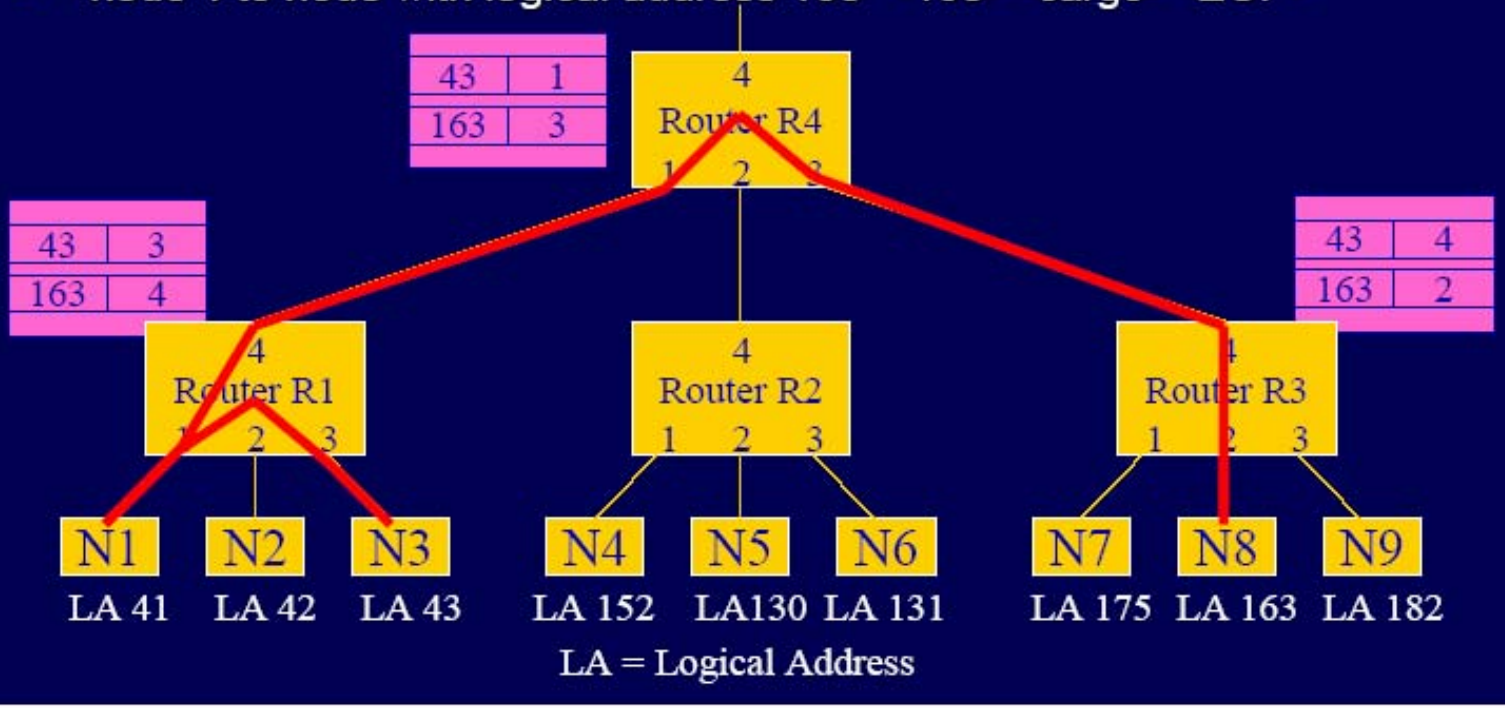
- destination is specified as router output port number
- node 1 to node 3 <3><cargo><EOP>
- node 1 to node 8 <4><3><2><cargo><EOP>



Steve Parkes 2003

Logical Addressing

- each destination has a unique logical address
- each router has a list of which port(s) to send data out for each possible destination
- node 1 to node with logical address 43 <43><cargo><EOP>
- node 1 to node with logical address 163 <163><cargo><EOP>



Steve Parkes 2003

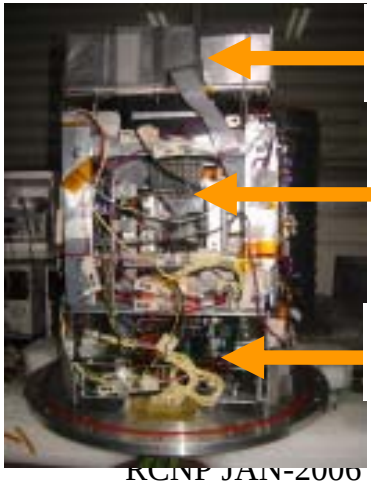
SpaceWire

- Remote Memory Access Protocol (RMAP)
  - RMAP is a protocol on the SpaceWire standard.
  - Register access has large overhead.
  - Block transfer works almost full speed.
  - It meets the requirements. Good enough.
  - PCI express and the other protocol may also meet the requirements. However, they may use too much logic (x10) for front-end FPGAs.

SpaceWire

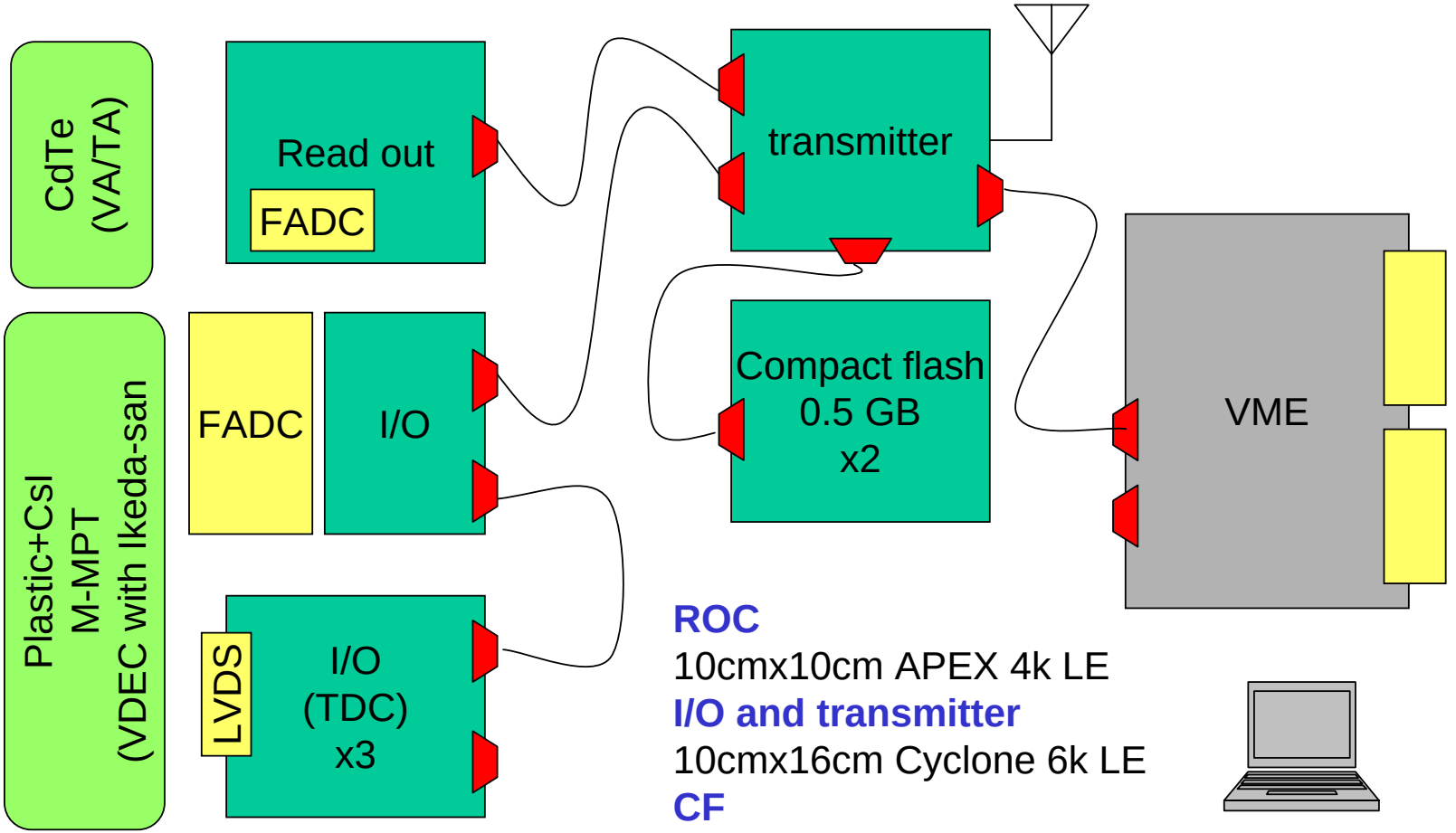
- SpaceWire自身は単なる「部品」。
- SpaceWireを用いたモジュラーなシステム設計。
- Hardwareからprotocolにとどまらず middle ware / architecture まで。
  - NIM moduleやCAMACが登場したときにアーキテクチャに与えたインパクトに匹敵

- 大気球実験の搭載機器などに展開
- Space Cubeと称したSpaceWire搭載の組み込み型コンピュータの開発



Balloon-borne electronics

Spacewire



ROC

10cmx10cm APEX 4k LE

I/O and transmitter

10cmx16cm Cyclone 6k LE

CF

10cmx16cm Cyclone 3k LE

Space Cube®

SpaceWire based computer developed by ISAS/ JAXA & Shimafuji.

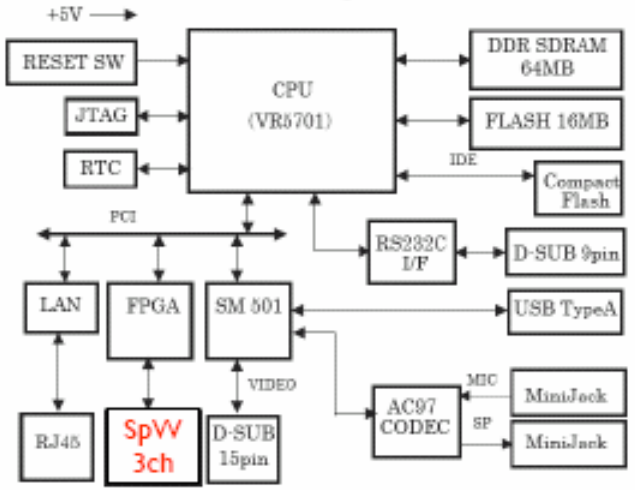
We are working on the standard SpW test system which allows us to skip interface testing of onboard equipments

: Send SpW commands

: Access by using RMAP

: can be used as a standard EGSE

Block Diagram



Specification

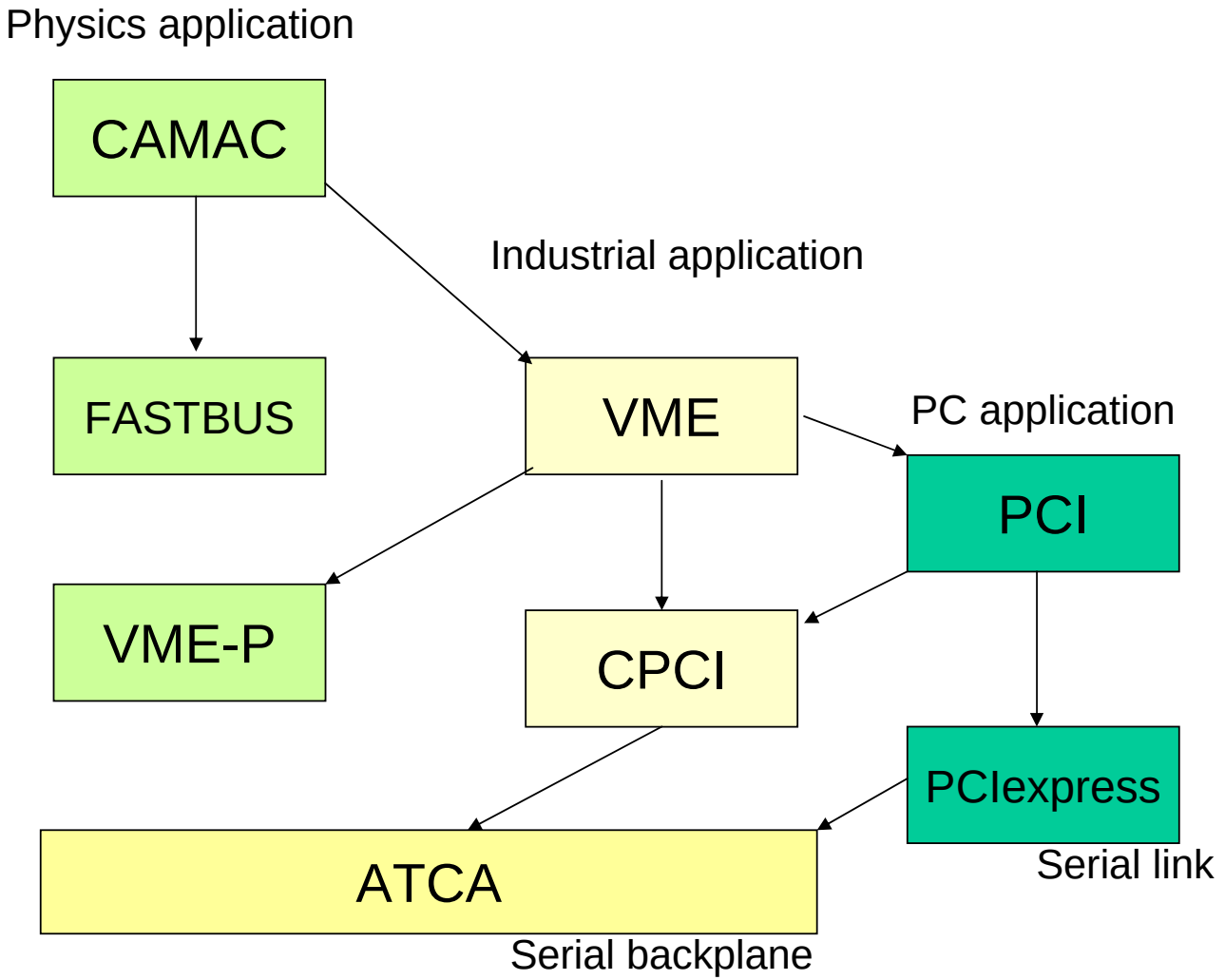
CPU	VR5701 200MHz／250MHz／300MHz
FlashROM	16M Byte
DRAM	DDR SDRAM 64M Byte
INPUT/ OUTPUT	IEEE1355 (SpaceWire), RTC, CF (True IDE), XGA (1024×768), USB1.1, LAN (100BASE), Audio (Stereo) RS232C, JTAG I/F (Debug)
POWER	+5V
SIZE	52mm×52mm×55mm

Data BUSを使わない、Flexibleなconfiguration

SpaceWire付きモジュール

1) NIM trigger module (Scalar/TDC/etc.)
2) 14bitt FADC
3) 12bit FADC(20MHz)
4) LVDS I/O module
5) VME logic board
6) VA/TA readout
7) ……
And Advanced TCA

History


Physics application
CAMAC
FASTBUS
Industrial application
VME
VME-P
CPCI
PC application
PCI
PCIexpress
Serial link
ATCA
Serial backplane

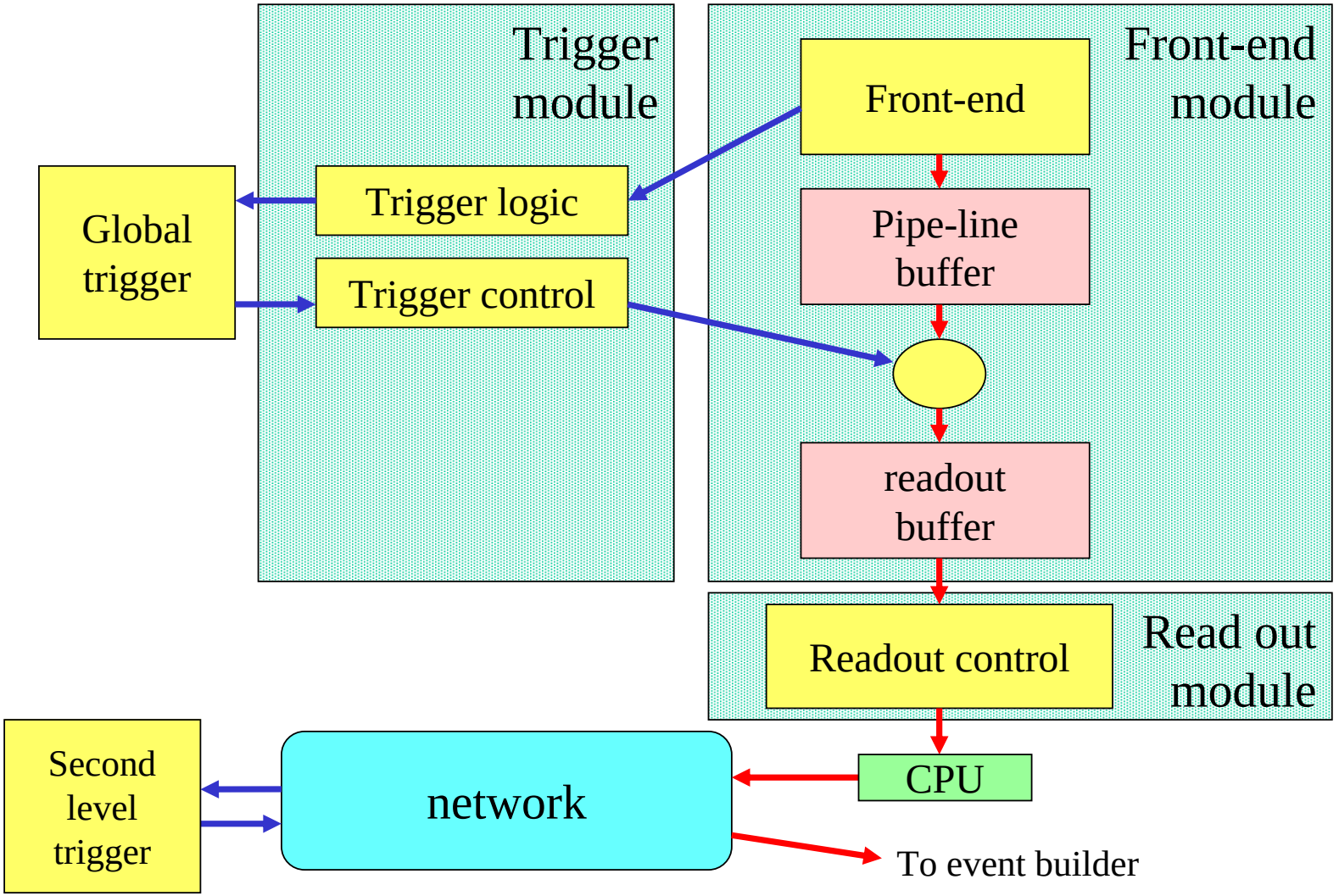
Mechanical Configuration

- 8U boards in 12U chassis
  - 16 slots in 600 mm frame
  - 14 slots in 19" cabinet
- 1.2" board pitch allows heat sinks plus rear SMT
- Forced air cooling for up to 200 watts per slot
- Front and rear fiber bend area in 600 mm depth
- Simplified sheet metal construction
- ETSI & NEBS vibration, shock and serviceability

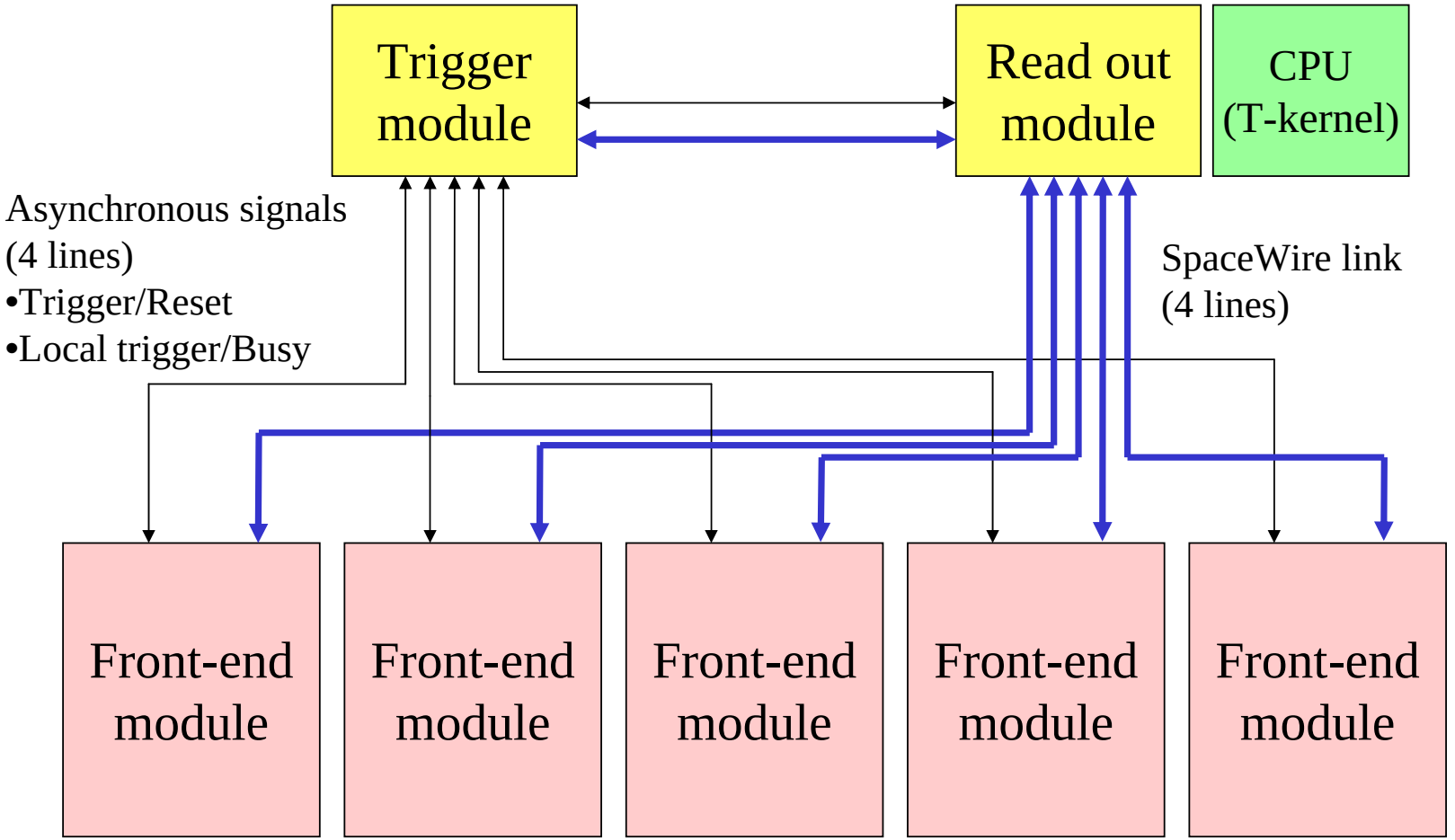
Advanced TCA

- Features
  - -48V DC power supply and on board DC converter for any voltages required.
  - 8U x 280 mm
  - Dual Star point to point differential connection
  - No definite protocol.
    - VME back plane is for VME protocol. While, ATCA back plane is only defined as 100 ohm differential. Any protocol can use ATCA back plane. (for example, ATCA for physics instrumentation)

DAQ system


Trigger module
Front-end module
Front-end
Trigger logic
Global trigger
Trigger control
Pipe-line buffer
readout buffer
Readout control
Read out module
Second level trigger
network
CPU
To event builder

Dual star connection



ATCA crate

One crate holds 96ch of 500MHz FADCs.
Total power is expected to be 260 W.

Trigger module

16 LVDS in
16 LVDS out
8 NIM in
8 NIM out

Power consumption is about 10W

Cyclone EP1C12 for trigger logic
Cyclone EP1C6 for SpW
100Mbps SpW

500 MHz FADC

8 ch analog input FADC mezzanine card is developed at KEK
(FINESSE format)

Power consumption is About 20W

Cyclone EP1C6
Cyclone EP1C12 for router
100Mbps SpW (8~9 MB/s from the module)
Readout buffer with 128Mb SDRAM waiting second level trigger

Summary

- SpaceWire Remote Memory Access Protocol provides compact and flexible interconnection in a module and inter-module connection.
- Advanced TCA provide dual star LVDS connections. They are good to be applied for DAQ system
- Downsizing may continue.
  - We might have another solution in the future.