RCNP研究会

マイクロパターン検出器の開発と展望

RHIC PHENIXにおけるPIXEL検出器の開発

理化学研究所　延與放射線研究室
小貫良行

PHENIX/VTX group

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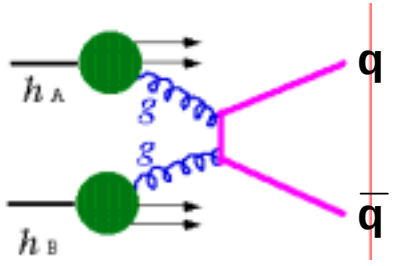
Spin physics

Only 1/4 to 1/3 of the proton spin is carried by quarks.

$$\frac{1}{2} = \frac{1}{2}\Delta\Sigma + \Delta G + L$$

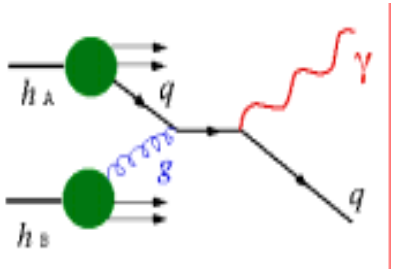
Investigating nucleon spin structure by polarized proton-proton collider to utilize quark/gluon as probe, instead of lepton DIS.



$$A_{LL} = \frac{\sigma(++) - \sigma(+-)}{\sigma(++) + \sigma(+-)} \approx \frac{\Delta G}{G}\frac{\Delta G}{G} a_{LL}(gg \to q\bar{q}X)$$

Observable ***Gluon polarization*** ***pQCD calculation***

→Heavy flavor identification



$$A_{LL} = \frac{\sigma(++) - \sigma(+-)}{\sigma(++) + \sigma(+-)} \approx \frac{\Delta G}{G}\frac{\Delta q}{q} a_{LL}(gq \to X\gamma)$$

γ+ jet event

→large acceptance detector

QGP physics

QCD energy loss and Debye screening in QGP depends on flavor.

- **Production cross section of quarkonium such as J/ψ ,ψ' in QGP are suppressed via gluon dissociation.**
- **R_{AA} measurement for open charm and bottom.**

With tight displaced vertex cut
- Separate c and b
- Separate B→J/ψ →ee and prompt J/ψ

With loose vertex cut to reduce light meson decays
- Reduces background in open charm measurements
- Reduces combinatorial background in quarkonium

Improved momentum resolution
- J/ψ and ψ' separation
- Upsilon states separation

→Heavy flavor identification
→Displaced vertex

Requirements for VTX

Physics side

- **High precision tracking for displaced vertex measurement.**
  40μm displaced vertex resolution, cτ =123μm(D^0), 460μm(B^0)
- **Large coverage tracking capability with momentum resolution**
  (|η|<1.2 , and full azimuthally with σ/P ~ 5%P)

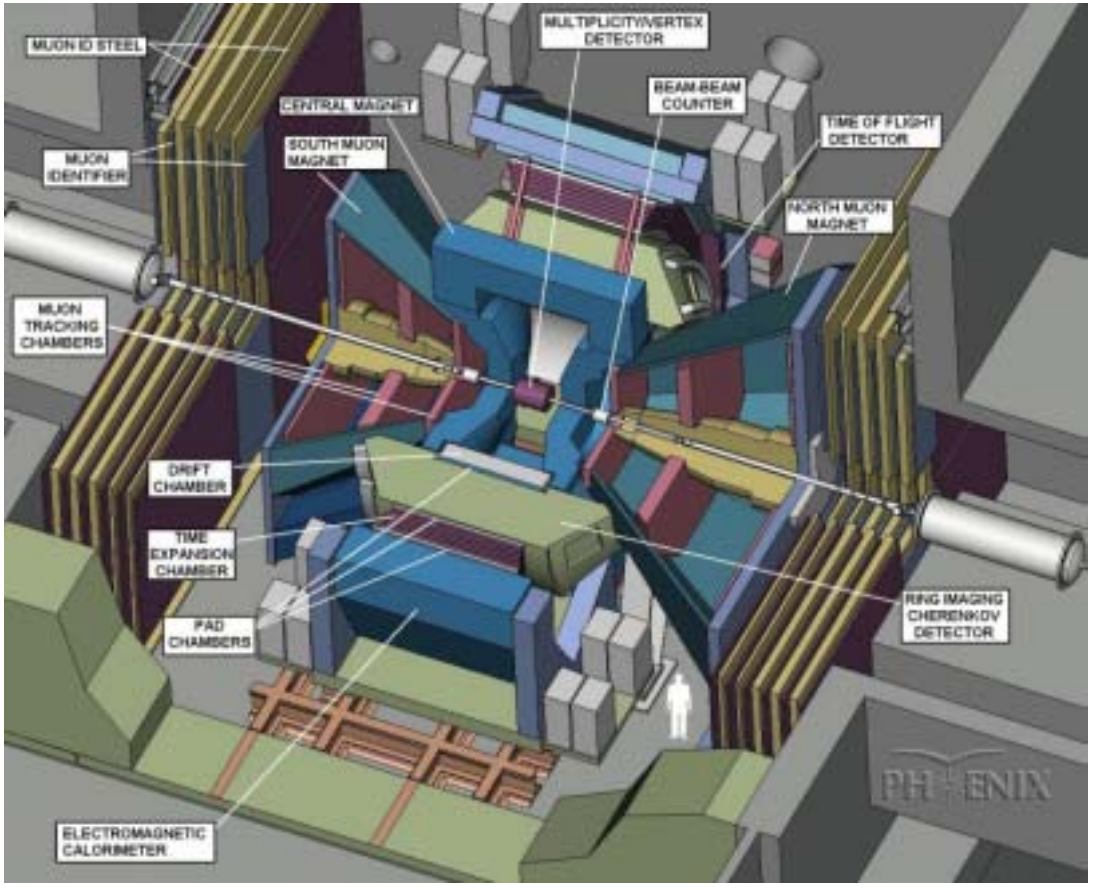
Environment side

- **High charged particle density dN/dη ~ 700 @η=0 (Au-Au)**
- **High Radiation Dose ~100KRad@10Years**
- **High Luminosity $2\times10^{32}cm^{-1}s^{-1}$@pp**
  Level 1 trigger rate ≤ 25 kHz @PHENIX-DAQ
  readout all data in ~ 40 μs
- **Low Material Budget 1.2%/layer**
  Avoiding for multiple scattering/γ conversion

PHENIX Detector

The Pioneering High Energy Nuclear Interaction eXperiment

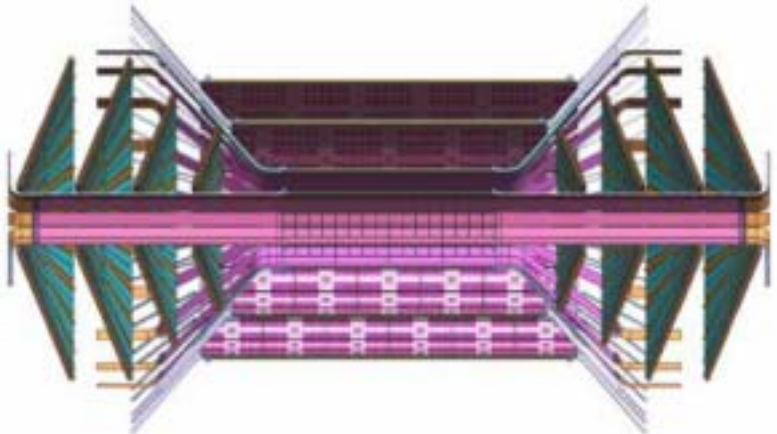
p, Au

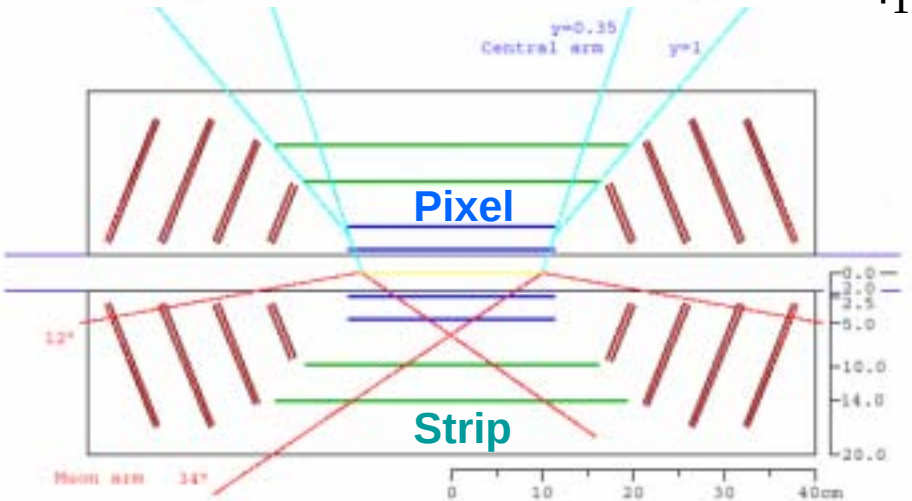


p, Au

- Good particle ID
- High resolution
- High trigger rate
- But not large acceptance

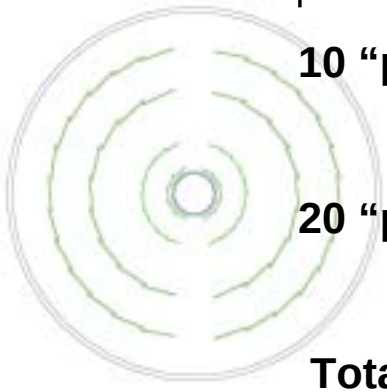
VTX Detector





- **Barrel region**
  - $|\eta|<1.2$, almost 2π in ϕ
  - Pixel sensor at inner 2 layers (r = 2.5, 5.0cm)
  - Strip sensors at outer 2 layers (r = 10.0, 14.0cm)
- **Forward region**
  - $1.2<|\eta|<2.7$, 2p in ϕ
  - 4 layers of mini strip (50 x 2000 to 11000 μm)
  - Trigger capable

Barrel in r-ϕ



10 “pixel-staves” in 1st layer

20 “pixel-staves” in 2nd layer

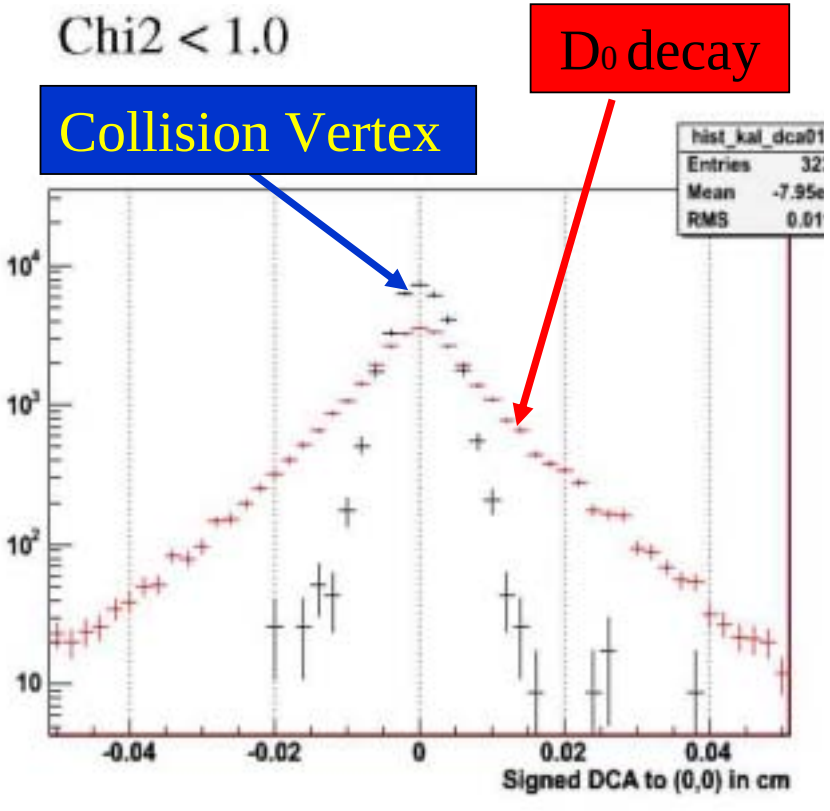
Total 30 pixel-staves

Hybrid type pixel sensor is adopted in PHENIX.
RIKEN pixel group is assigned to manufacture all staves.

Expected Performance

Layer	radius	Sensor	Occupancy	
Layer 1	2.5 cm	Pixel	**0.53 %**	
Layer 2	5.0 cm	Pixel	**0.16%**	
Layer 3	10.0 cm	Strip	**4.5 %** (x-strip)	**4.7 %** (u-strip)
Layer 4	14.0 cm	Strip	**2.5 %** (x-strip)	**2.7 %** (u-strip)

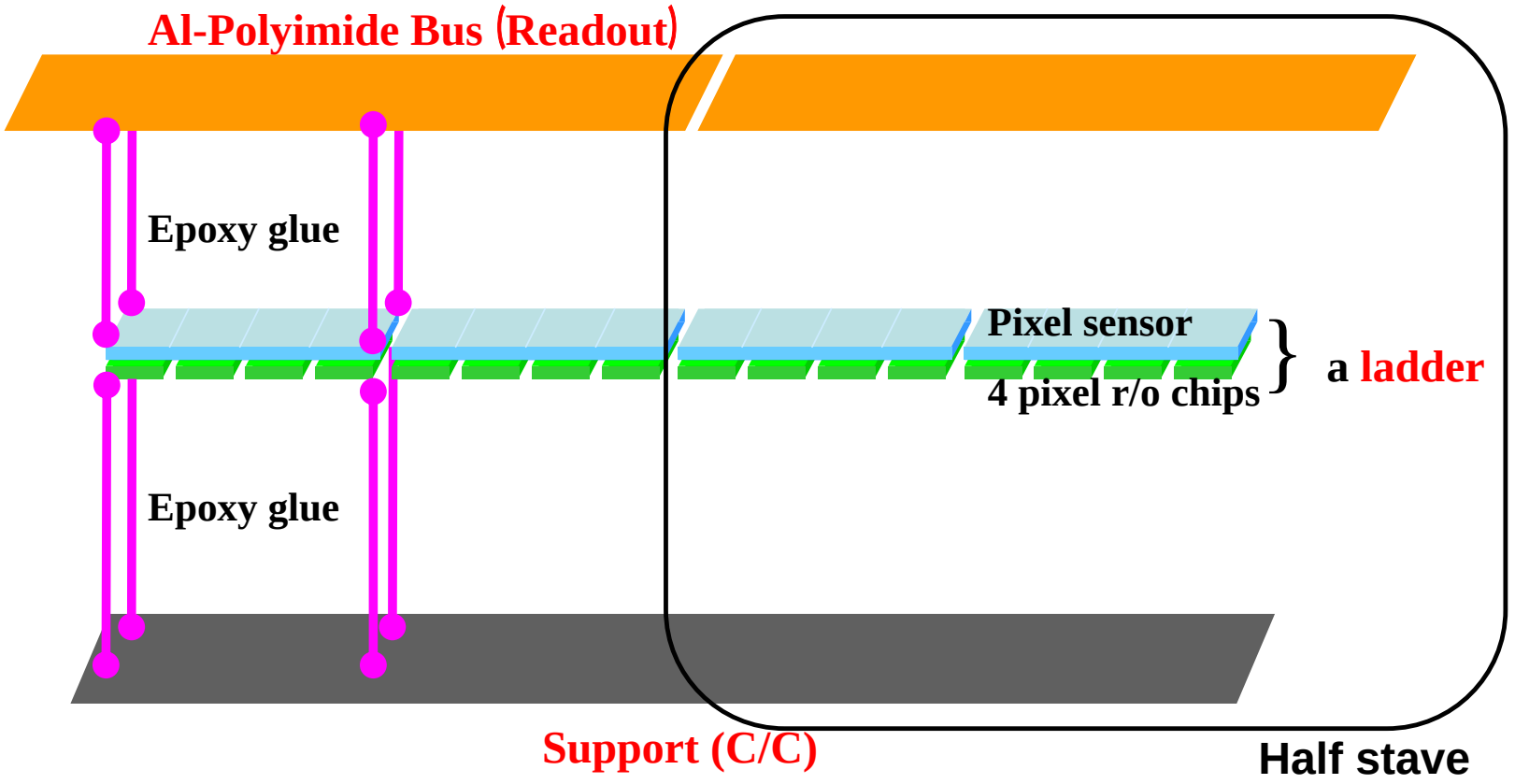
Expected occupancy at Au-Au 200GeV most central event



Distance to the Closest Approach [cm]

Au-Au central event

Components of pixel detector

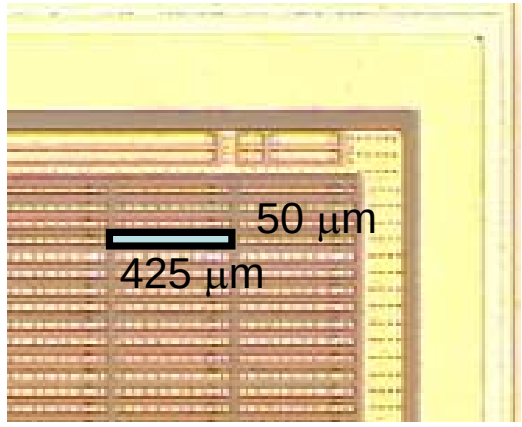


A full stave is consisted of 2 Buses + 4 ladders + 1 support.

A half stave is electrically independent from the other.

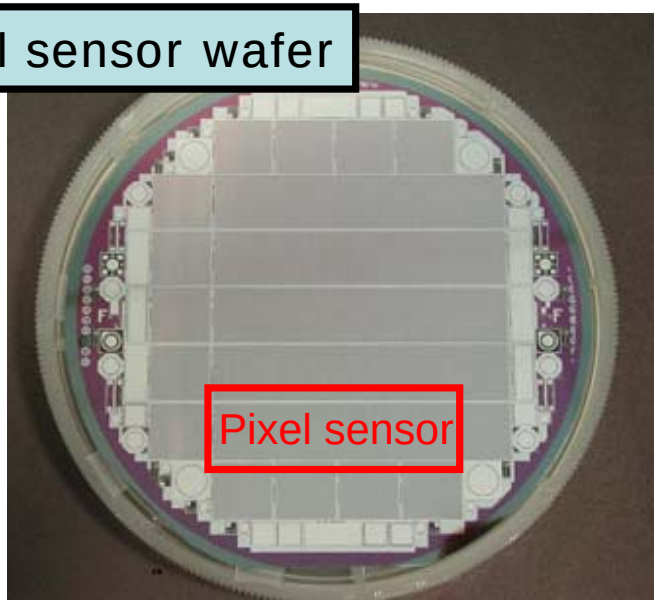
Pixel sensor

- p-in-n type silicon sensor (5” wafer)
- Thickness of the sensor is 200 μm
- 32 x 256 (x 4) pixels (8192 x 4 pixels)
- Pixel size match with size of cell in r/o chip
  - (50 x 425 μm^2)
- Active area : 12.8 x 13.6 mm^2
- Sensor bias voltage ~ 50V

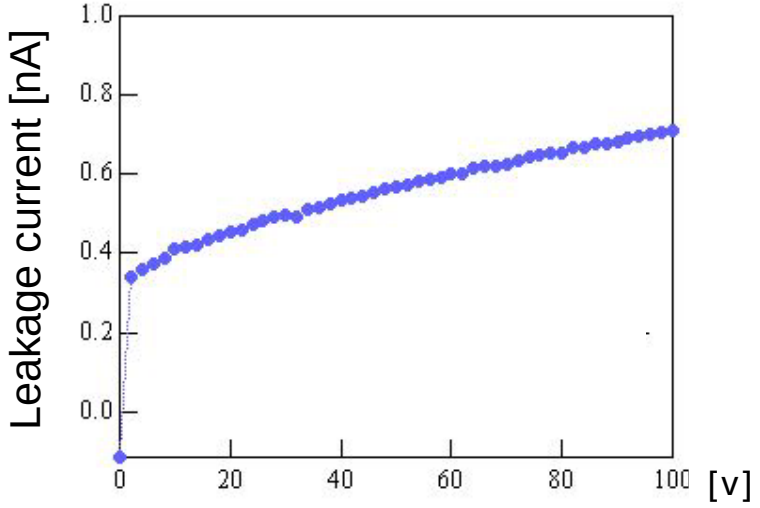


picture of a corner of a pixel detector sensor

pixel sensor wafer



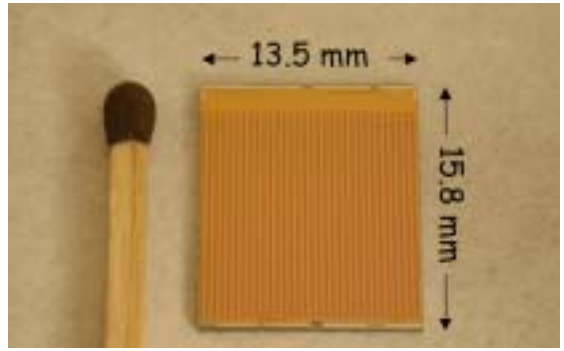
Layout of a 5” silicon sensor wafer

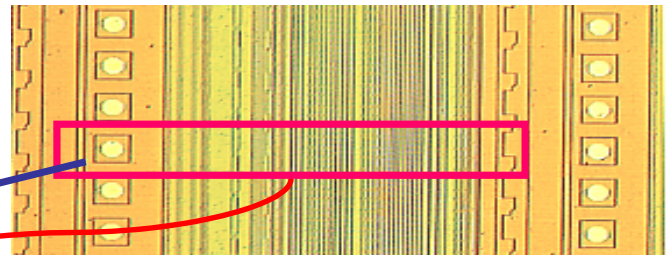


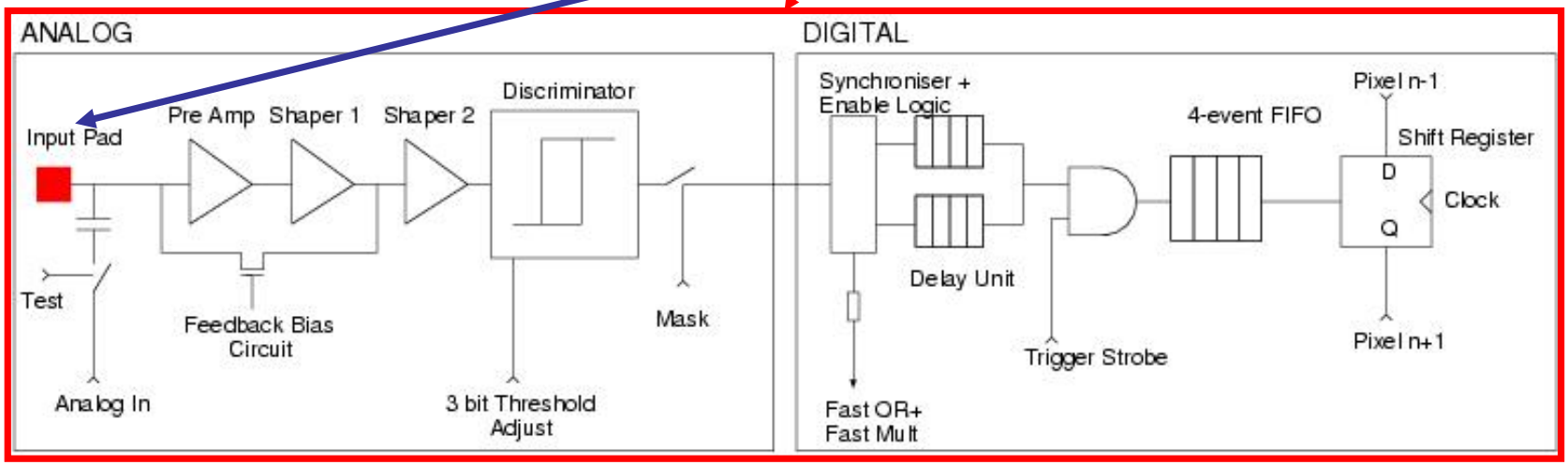
IV curve of the test diode structure on ladder wafer

Readout chip

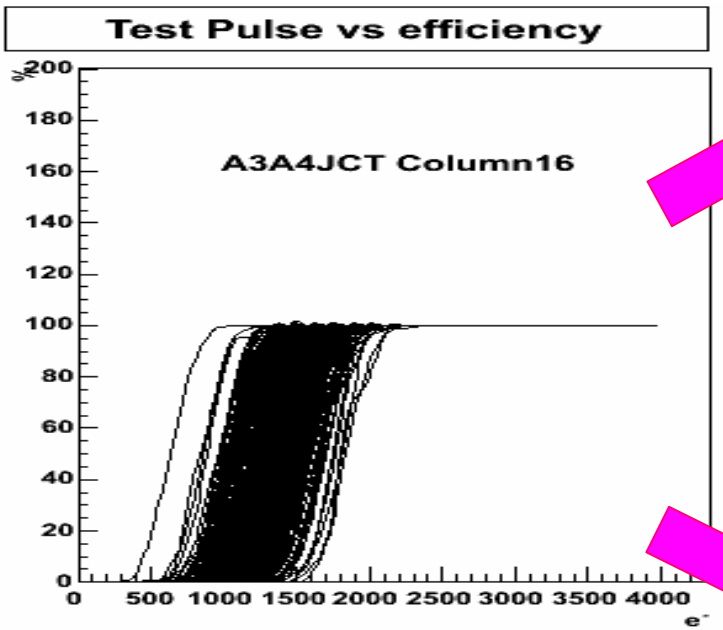
- **ALICE1/LHCB chip**
  - Chip size：13.5mm x 15.8mm x 150μm
    - (Active area: 12.8mm x 13.6mm)
    - CMOS 0.25 μm (8” wafers)
  - 8192 channels (32 x 256)
  - 4-event buffer; 10 MHz clock
  - radiation hard up to ~30 Mrad
  - ~1W/chip



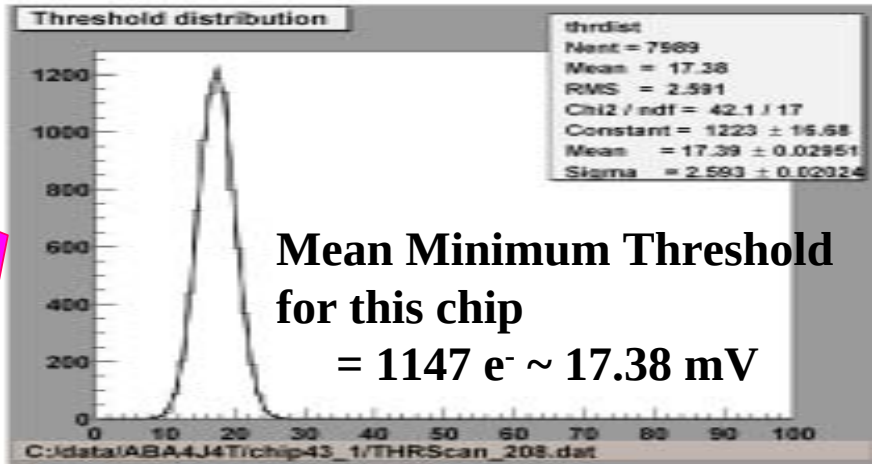




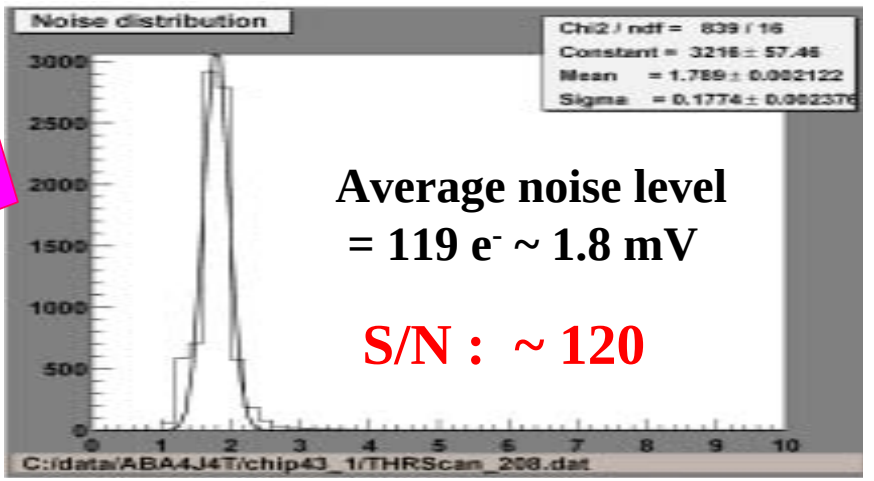
Threshold test for readout chip



Results of threshold scan for all individual pixel on column (256 curves are superimposed)



Mean Minimum Threshold for this chip
= 1147 e⁻ ~ 17.38 mV



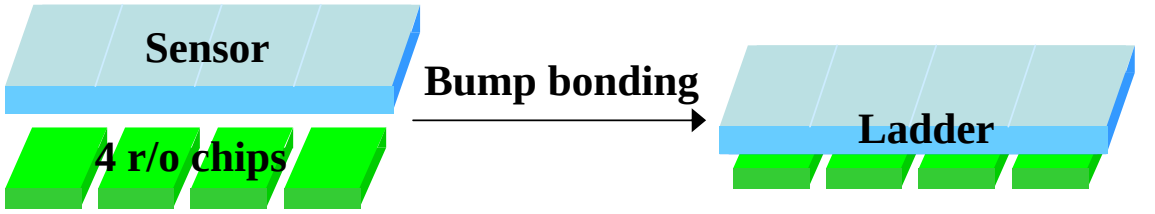
Average noise level
= 119 e⁻ ~ 1.8 mV

S/N : ~ 120

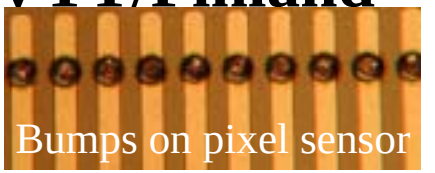
Minimum Ionization Particle signal in 200 μm sensor ~ 14,000 e⁻

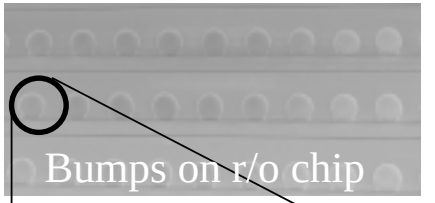
Bump bonding

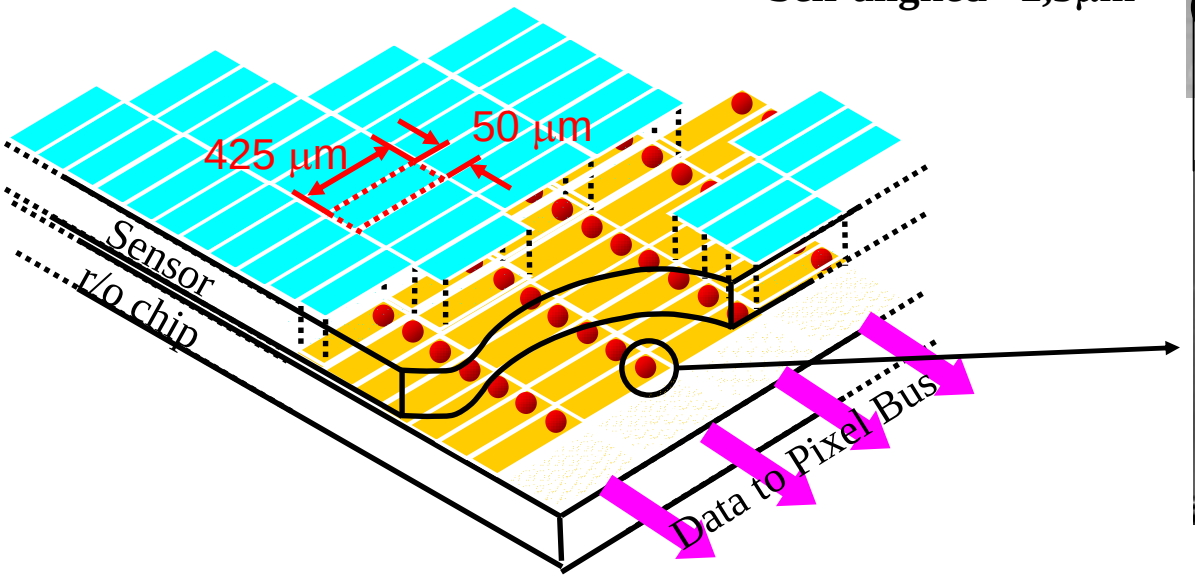
- **Readout chips are thinned down to 150 μm at VTT**
- **Interconnection with micro-soldering between pixel sensor and readout chips to be done by VTT/Finland**

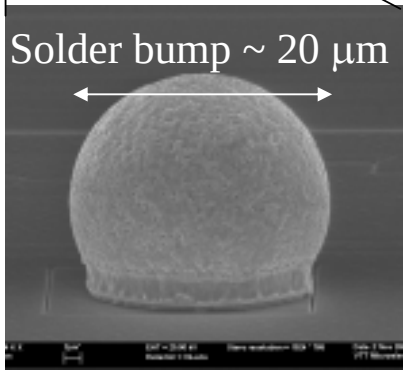


Self-aligned ~2,3μm

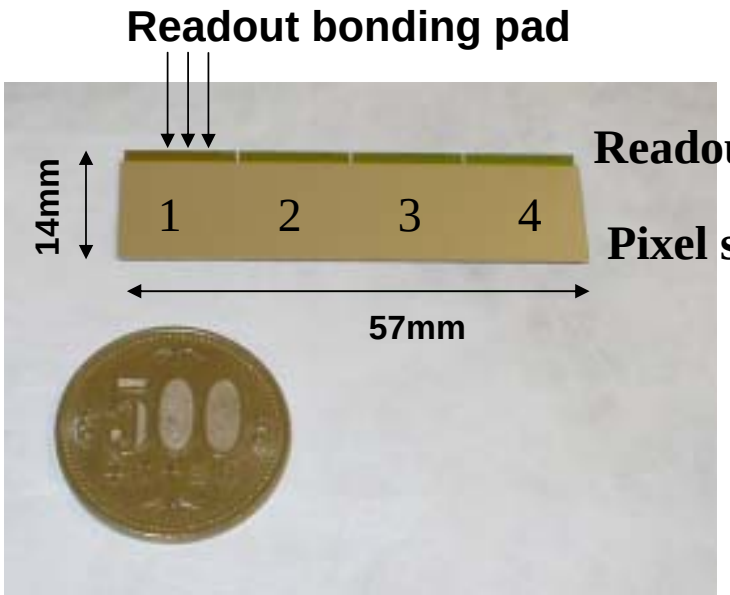


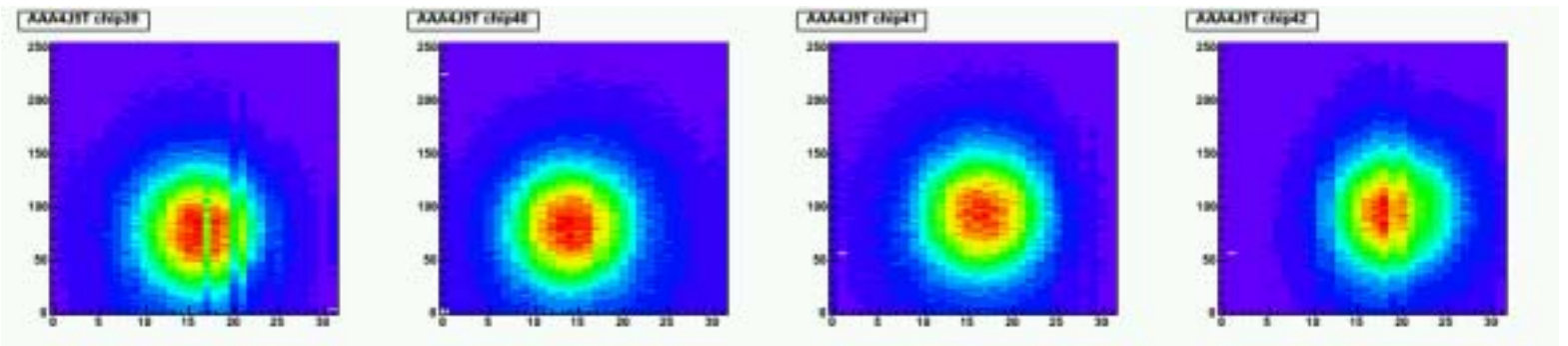






Source test



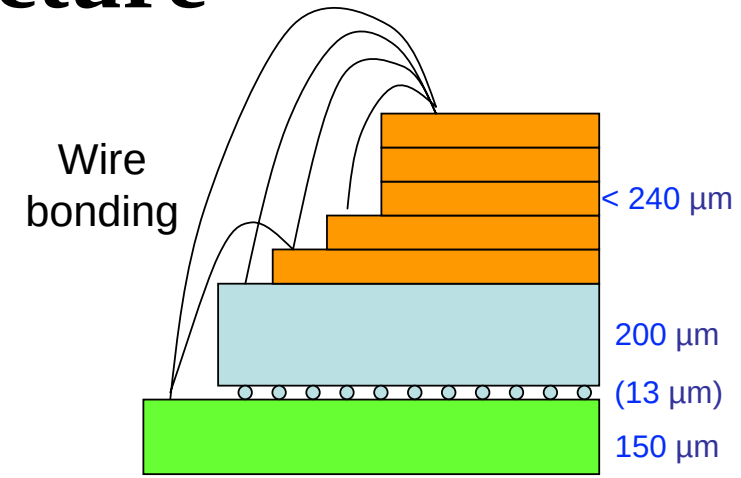


1 2 3 4

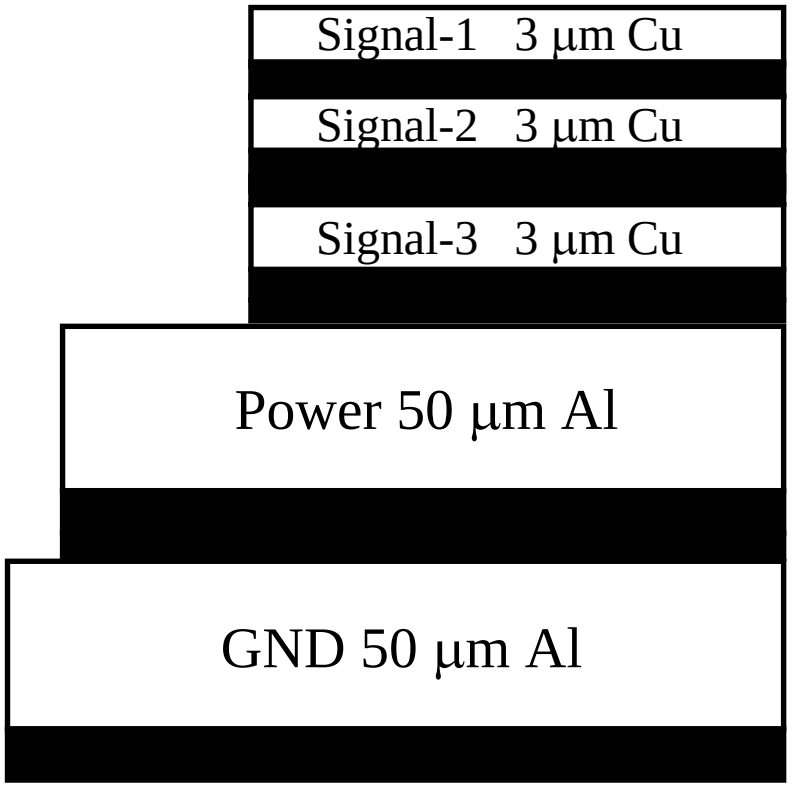
Hit map with β-source test

Bus structure

- **5 layers structure**
- **GND, Power and 3 signal lines**



Final planed



Signal 1; (for Surface Mount Device)

Signal-1 and Signal-2 is connected with through hole

Signal 2; (Vertical line)

line connected with pixel chip with wire bonding

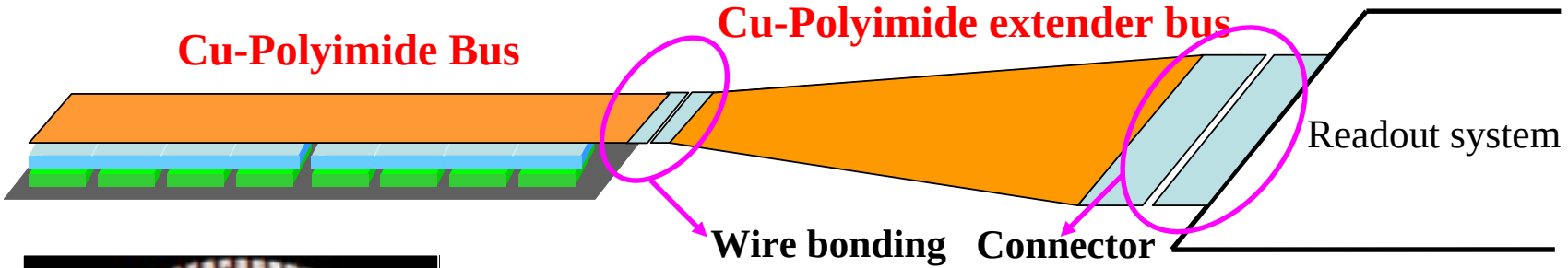
Signal 3; (Horizontal line)

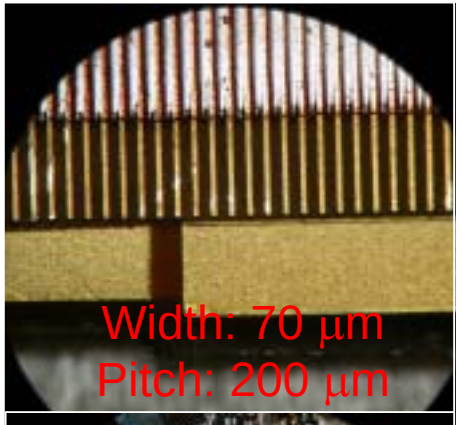
send signal to Pilot Module connected with vertical line with through hole

Line spacing; 70 μm pitch

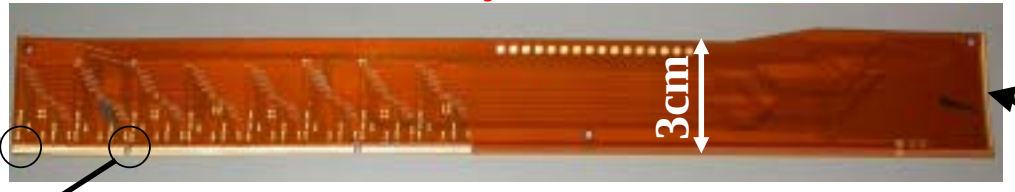
Material Budget; Total ~ 0.12 %

Cu-Polyimide test bus and extender bus

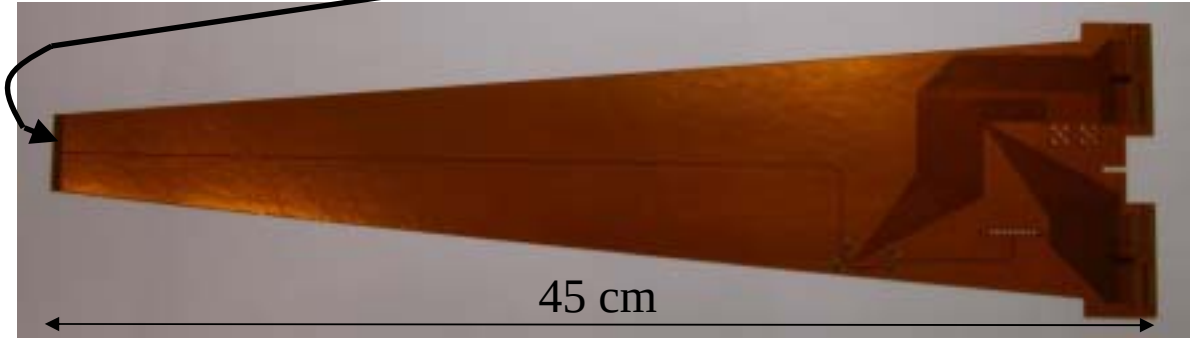




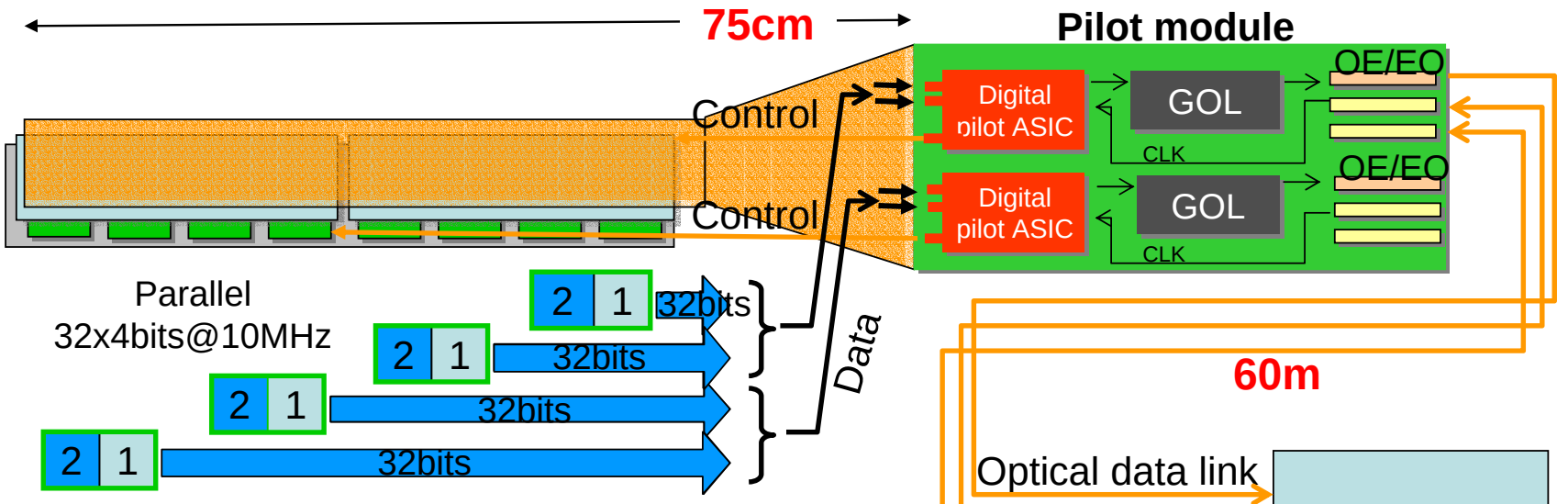
3cm Cu-Polyimide test bus



Cu-Polyimide extender test bus



Readout scheme

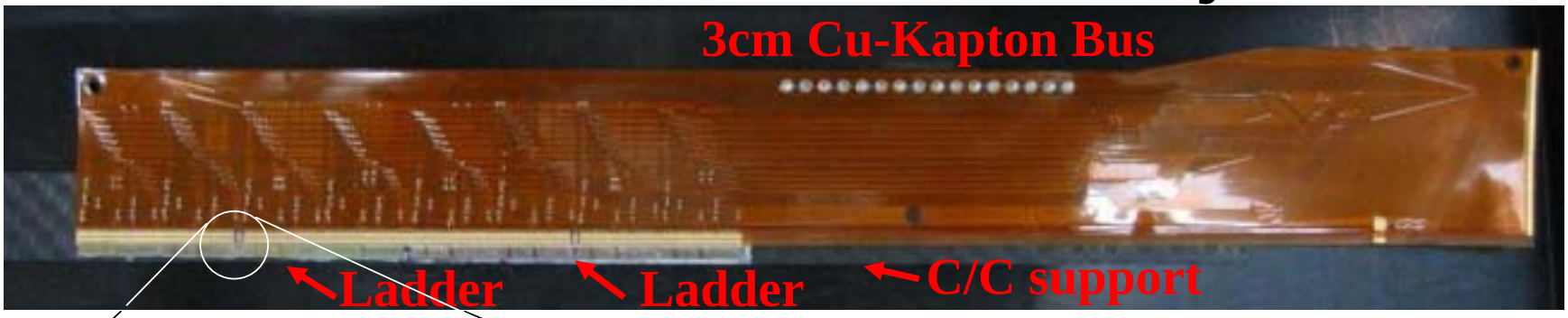


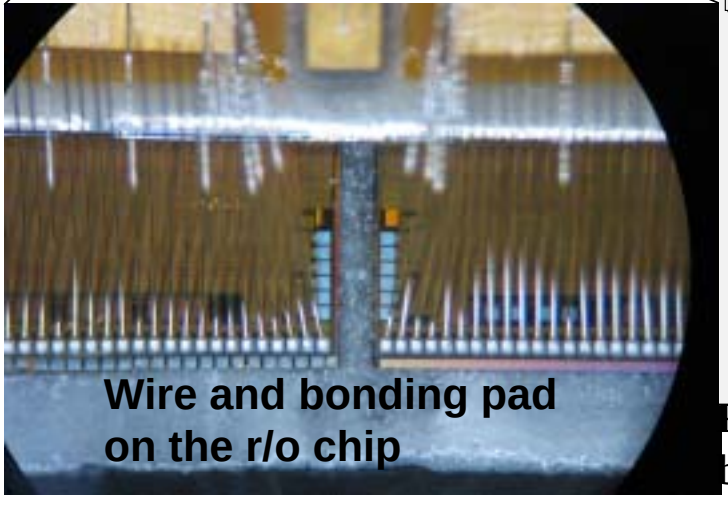
256 rows✕2 chips✕100 ns = **51.2 μs**

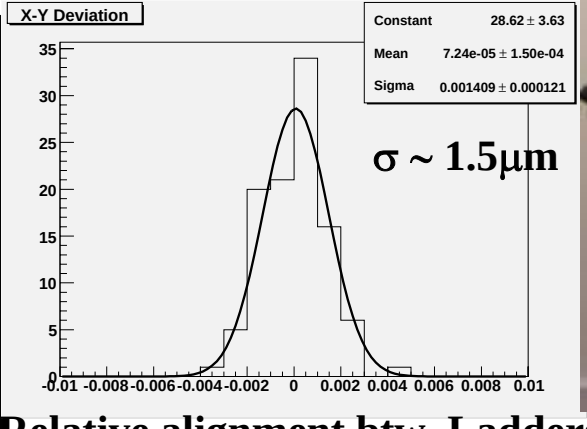
- **Digital pilot ASIC**
  - Sending commands to Pixel R/O chip
  - Receiving data from Pixel R/O chip
  - Send data to Front End Module
- **Gigabit Optical Link chip**
  - Serialize and transmit data with 1.6 Gbps
- **ANALOG pilot chip**
  - Supply reference volt. for Pixel R/O chips

Pilot module

First half stave assembly







Relative alignment btw. Ladders by 3D measuring machine (Borrowed from KEK-ATLAS)

Bonding machine owned by RIKEN

All assembly procedures are done by hand at Hayashi-Seimitsu Co.
Visual Inspection of wire-bonding was done and there were no problem.

Summary and Plan

- **The Silicon vertex tracker will be implemented into the PHENIX detector in 2009.**
- **R&D and Production are on going**
  - **Readout chip probing test**
  - **Ladder probing test**
  - **Development of readout bus**
  - **Development of readout system**
  - **Pixel stave assembly**
- **Second half stave will be assembled on Feb 6, 2006.**
- **First combined test with half stave and r/o system on Feb 15, 2006.**
- **Test beam on Spring 2006**