VERTEX2005 Conferenceの報告

KEK-IPNS

関本　美知子

VERTEX Conference とは・・・

- 第1回目のConferenceは、FinlandのBasto Islandで1992年に開かれた。この時はCERNのDELPHIなど約3つのプロジェクトに関して、誰でも（physicists, engineers, hardware, software…）参加し、フリップを使用して（no power!）議論された。
- 以後、世界の「water front」を会議の場として選びながら、毎年開催されてきた。

  （Slovenia, USA, Israel, Italy, Brazil, Greece, Netherlands, *USA, Switzerland, Hawaii, UK, Italy*）
- VERTEX2005は第１４回にあたり、

  Asiaでは初めて日本の日光中善寺湖畔で開催された。

Basto vs Nikko

Vertex 1992

A few detailed talks – physics, electronics..
Many questions and discussions
No summary or proceedings

Sauna & cold sea

Vertex 2005

Many talks – review + details
Some questions & discussions
Summary

Bath & cold wind

from Tyndel's summary

The VERTEX Series is International Workshop on Vertex Detectors

Emphasis is usually given to topics directly related to vertex detectors:

- **Vertex detectors at present experiments**
- **New vertex detector projects**
- **R&D for future vertex detectors**
- **Radiation hardness of detectors and R&D on new materials**
- **Radiation hardness of integrated readout electronics**
- **DAQ and trigger architecture for vertex detectors**
- **Vertexing algorithms and performances**
- **Applications of vertexing instrumentation to other fields.**

Additional talks usually available for new and innovative ideas and applications.

VERTEX2005@ *Lakeside Hotel, Chuzenji Lake, Nikko*

Local Organizing Committee: **Chair; A. Miyamoto (*KEK*), J. Haba (*KEK*), Y. Unno (*KEK*), Y. Sugimoto (*KEK*)**

- **参加者：外国から35人、日本から15人**
- **日程：** 2005.11.7 9:00 ～ 11.11 12:00

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- **日程＆報告数：**2005.11.7 9:00〜11.11 12:00
  40**件（各30分**or20**分）**
- **報告された研究所＆グループ、他分野：**

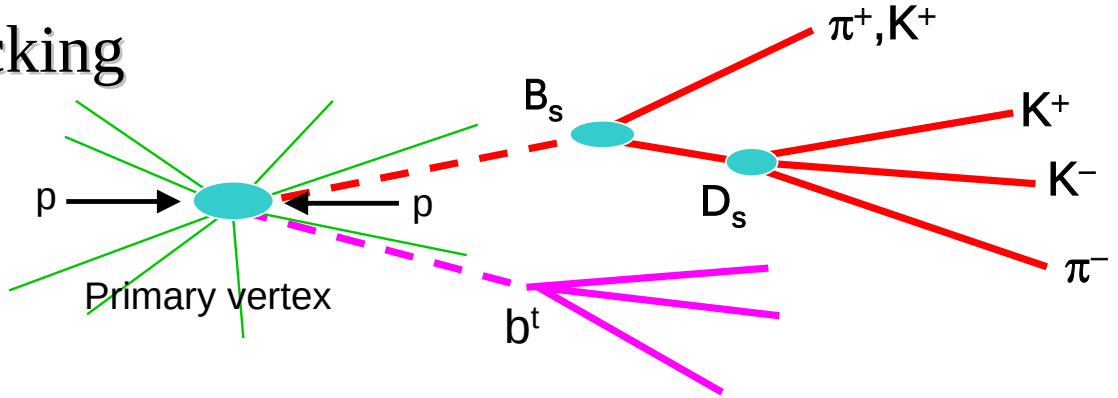
KEK; *BELLE*, *K2K*(*T2K*)
CERN; *ATLAS*, *CMS*, *LHCb*, *ALICE*, **DESY**; *ZEUS*
FNAL; *D0*, *CDF*, **SLAC**; *BaBar* **BNL**; *PHENIX*
future projects; *ILC*, *S-LHC*, *S-Bfactory*
other fields; **医学、核融合、宇宙、放射光**

何が報告されたか？

- 7 operating experiments
  - each with 1-3 Si technologies
  - Most with upgrade plans
- 11 projects under construction
- 20 RD efforts or specialised techniques
- 4 from other fields

from Tyndel's summary

Vertexing & tracking



1. Measure the first point precisely (1 or 2D) & with 'no' material
   -- Material perturbs trajectories θ (mrad) ~ 1.4*sqrt (tX0(%)/p(GeV))

2. Measure the angle precisely
   -- Goal is that the multiple scattering in the beam pipe/first layer should dominate i.e. s ~ 1mrad

3. Measure the curvature
   -- Precision ~ L2. Value is driven by physics (charge ID; mass resolution)

4. …and cover a large solid angle

- In principle simple but in detail complicated (as we have heard) !

Silicon system performance

- *I had thought to gather and compare performance figures. Impossible & probably of no use. Much more fun (for me and you) to collate problems and ideas & try and learn lessons.*

	Typical values today
• Resolution - σ_{rf} σ_z	< 10mm
• Granularity or cell size	20x20mm^2 (CCD, APS, DF)
	0.02 mm^2 (pixels)
Missing short strips/macro-pixels ➔	10.0 mm^2 (strips)
• FE Speed & noise	25nsec, S/N ~ 20
• Power/channel (1msec – 25nsec)	1 ~ 5mW (strips LC-LHC)
	0.1mW(pixels);
	0.1mW(CCDs)
• Material in X0	1%(strips); 2%(pixels)
• Geometry and sImpact	< 20mm from beam; ~20mm
	b-tags and some c-tag?
• Efficiency	99%(build) – 85%(running)

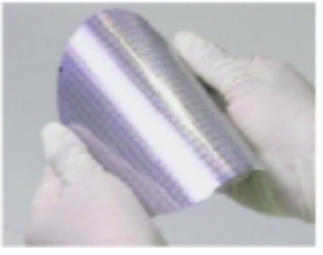
VERTEX2005@ *Lakeside Hotel, Chuzenji Lake, Nikko*

Local Organizing Committee: A.Miyamoto(Chair), J.Haba, Y.Sugimoto, Y.Unno

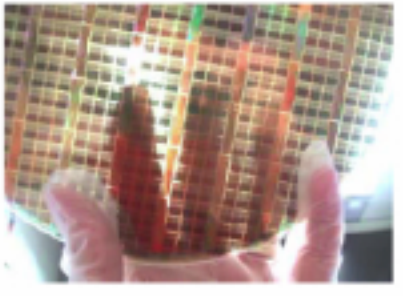
- 詳しくは、*http://www-conf.kek.jp/vertex2005* のプログラムを参照してください。
- 特に、M. Tyndel (RAL)の*Summary* によくまとめられています。
- また、R. Yarema (Fermilab)がElectronicsの立場からHEPの将来計画にむけてまとめられています。

Wafer Thinning

- Detectors and readout chips make a significant contribution to multiple scattering
  - Every 100 μ of silicon is 0.1% X_0
  - Hybrid pixels have 2 layers of silicon, each greater than 100 μ thick
- Take advantage of work being done in industry by major companies (IBM, INTEL, Toshiba, etc.) to reduce wafer thickness
- Thinning
  - Thinning to 50 microns is in production
  - State of the art – CMOS wafers thinned to 10-15 microns by lapping/grinding followed by wet or plasma etch and CMP. Thinner for SOI.
- Challenges
  - ***Handling/breakage***
  - ***Thickness uniformity on large wafers***
  - ***Circuit performance changes due to thinning***
    - ***No change in Vt for 25u wafer (Fraunhofer, IZM)***
    - ***No change in Idsat for 25 u wafers (IZM)***
    - ***More tests needed***

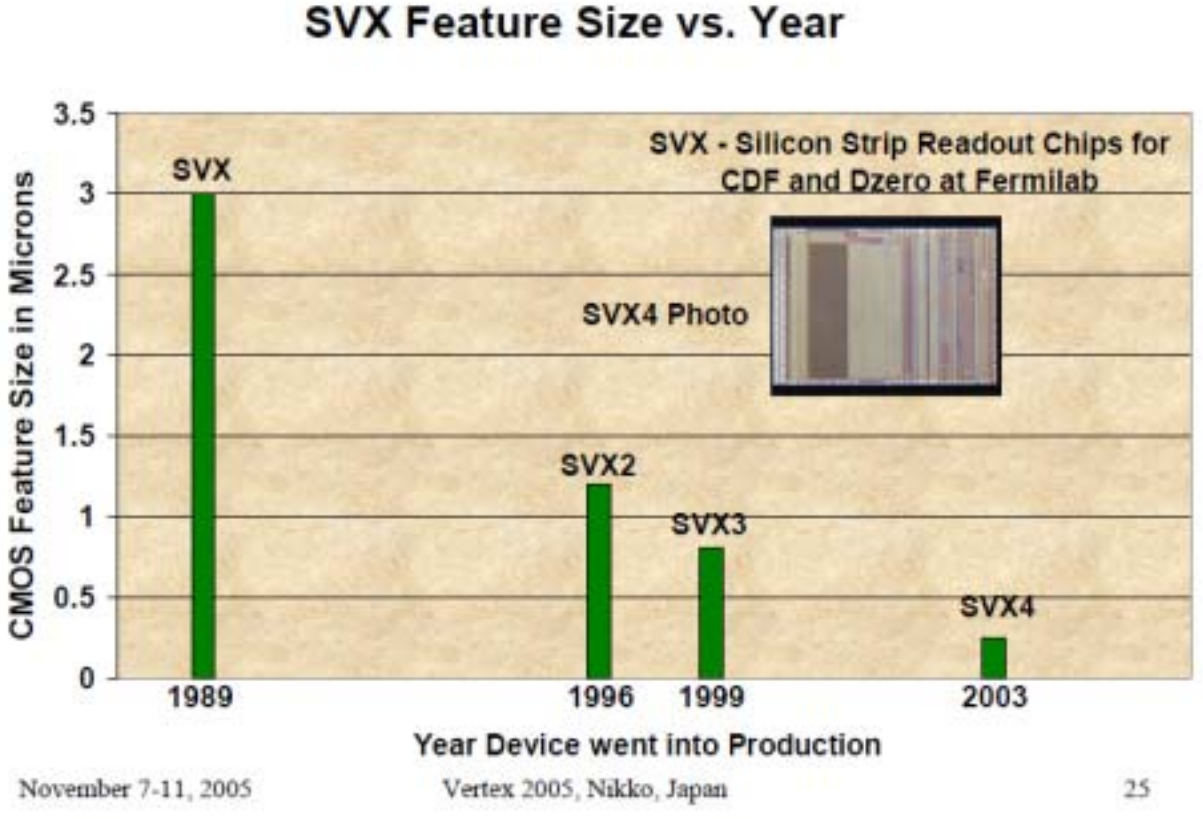


Thinned IC wafer (J. Joly, LETI)

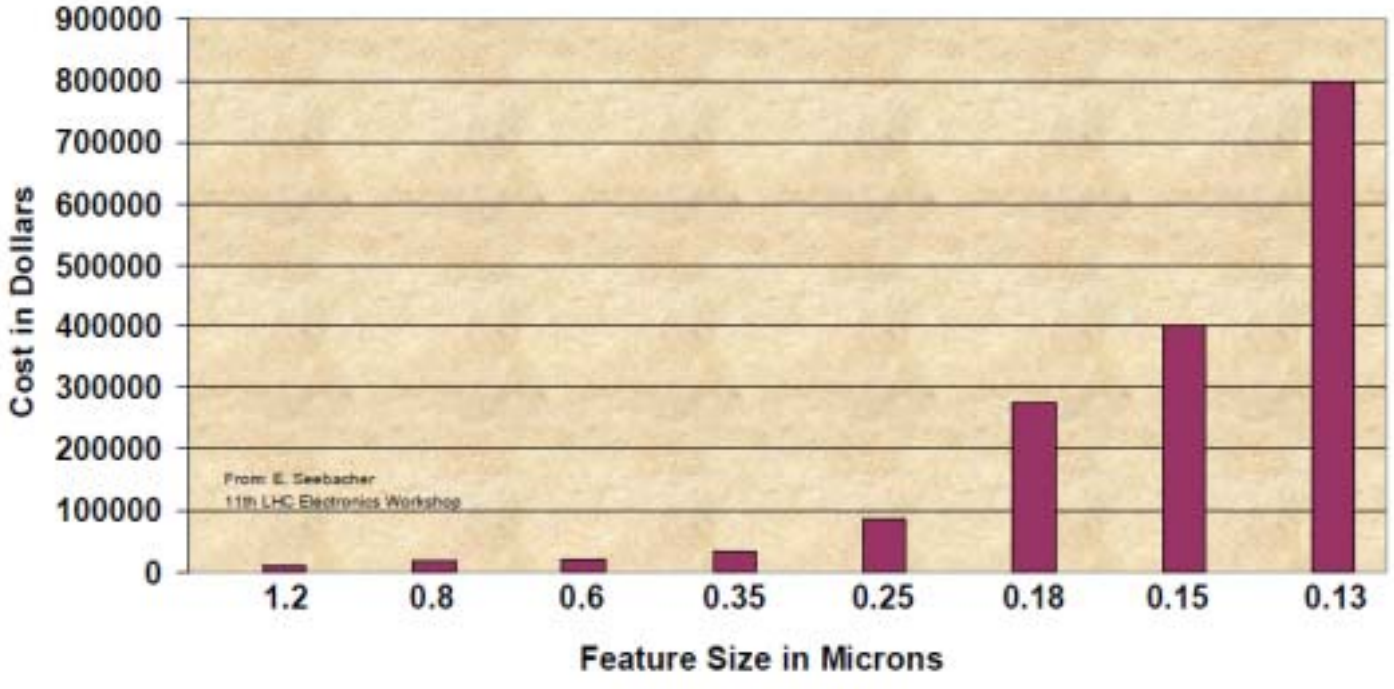


Thinned 200 mm wafer transferred on to glass handle wafer (A.Young, IBM)

CMOS Feature Size Decrease



Mask Cost for CMOS Processes



November 7-11, 2005 Vertex 2005, Nikko, Japan 28

Challenges and the Future

- Technology tradeoffs must be made depending on the application.
- As a general rule good tools and experienced designers will reduce the number of design iterations saving development time and overall cost.
- A few questions to think about
  - What is the proper balance between on chip regulation (higher power dissipation) with the potential reduction in cabling mass and power?
  - Will special design rules still be necessary at smaller CMOS features sizes, or at what level will the special design rules be necessary
  - Will wafer thinning and 3D circuits become practical for HEP
  - Can power ramping be made to work in future very large systems
    - Readout stability
    - Thermal cycling
    - Pickup
  - Can analog information be given up to reduce system complexity and reduce power dissipation?
  - Can designs be tested in larger feature sizes to save development money
    - Similar thing was done before with rad soft to rad hard design process.
- Many questions – lots of work to be done
- Start thinking now - the future is just around the corner

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- また、R. Yarema (Fermilab)がElectronicsの立場からHEPの将来計画にむけてまとめられています。
- 「高エネルギーニュース」最新号（今月配布？）に、講演者とその簡単なトピックをまとめたものが報告されています。個々の講演を検索する参考にしてください。

検出器製作において参考になる

(関本が捉えた) keywords

I. Radiation-hardness
II. Humidity
III. Kapton Technology

I. Radiation-hardness

- Review all components for radiation hardness
  - Include all ASICs, opto-links, glues
- Build in radiation & beam loss monitors
  - There is a lot of energy in beams
    - Can cause **physical damage**
    - Results in damage to
      - Silicon (pinholes in Belle)
      - ASICs (many expts)
      - Power supplies (CDF)…
  - **Diamonds** are now available as BCMs

I. Radiation-hardness

- **Belle: Luminosity ($1.6\times10^{34}cm^{-1}\cdot s^{-2}$) ×3 @ 2007**
  → トリガー系のupdate

  ×30 @ Super-B → monolithic active pixel sensor
  continuous acquisition pixel (CAP)

- **ATLAS: 集積 Luminosity ~ 3000 fb^{-1} @ SLHC**
  → diamond pixel detector

- **Czochralski silicon: 耐放射線の強いシリコン（結晶の成長方法による違い）**

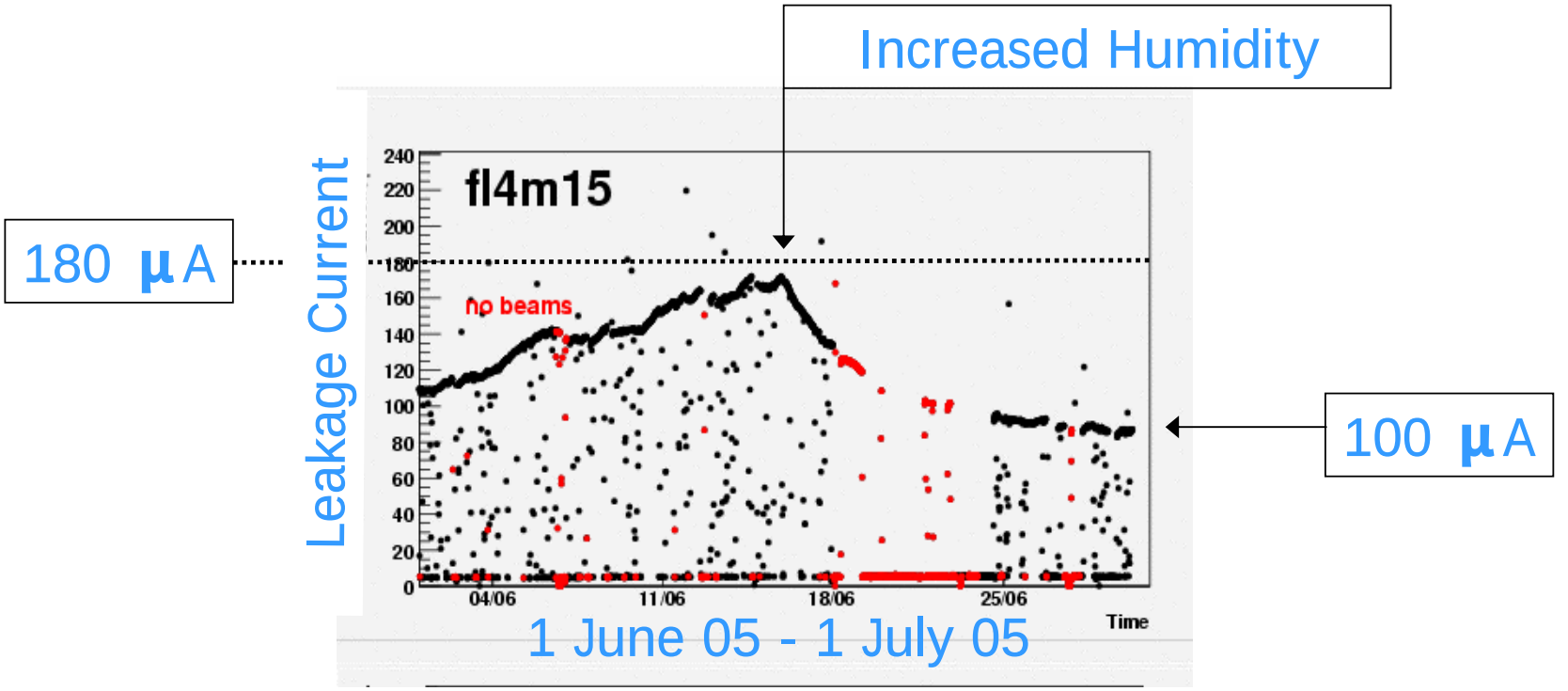
- and ‘‘‘‘ of course, future big projects, not only HEP but also NP and others needs the new technologies for radiation-hardness

II. Humidity

- **Surface charge: depend on humidity, temp**
  Micron detectors in BarBar
- **Leakage current: more humidity helps to stop the effect**
  "Humidity plays a role"

Leakage Current Increase

Using humid air and a new reference voltage setting, the **situation now is under control**



II. Humidity

- **Surface charge: depend on humidity, temp**
  Micron detectors in BarBar
- **Leakage current: more humidity helps to stop the effect**
  "Humidity plays a role"
- **Corrosion:**

  CMS discovery that Humidity reacts with Phosphorus (present in a 4% concentration into the passivation oxide) and forms an acid that corrodes Aluminum.

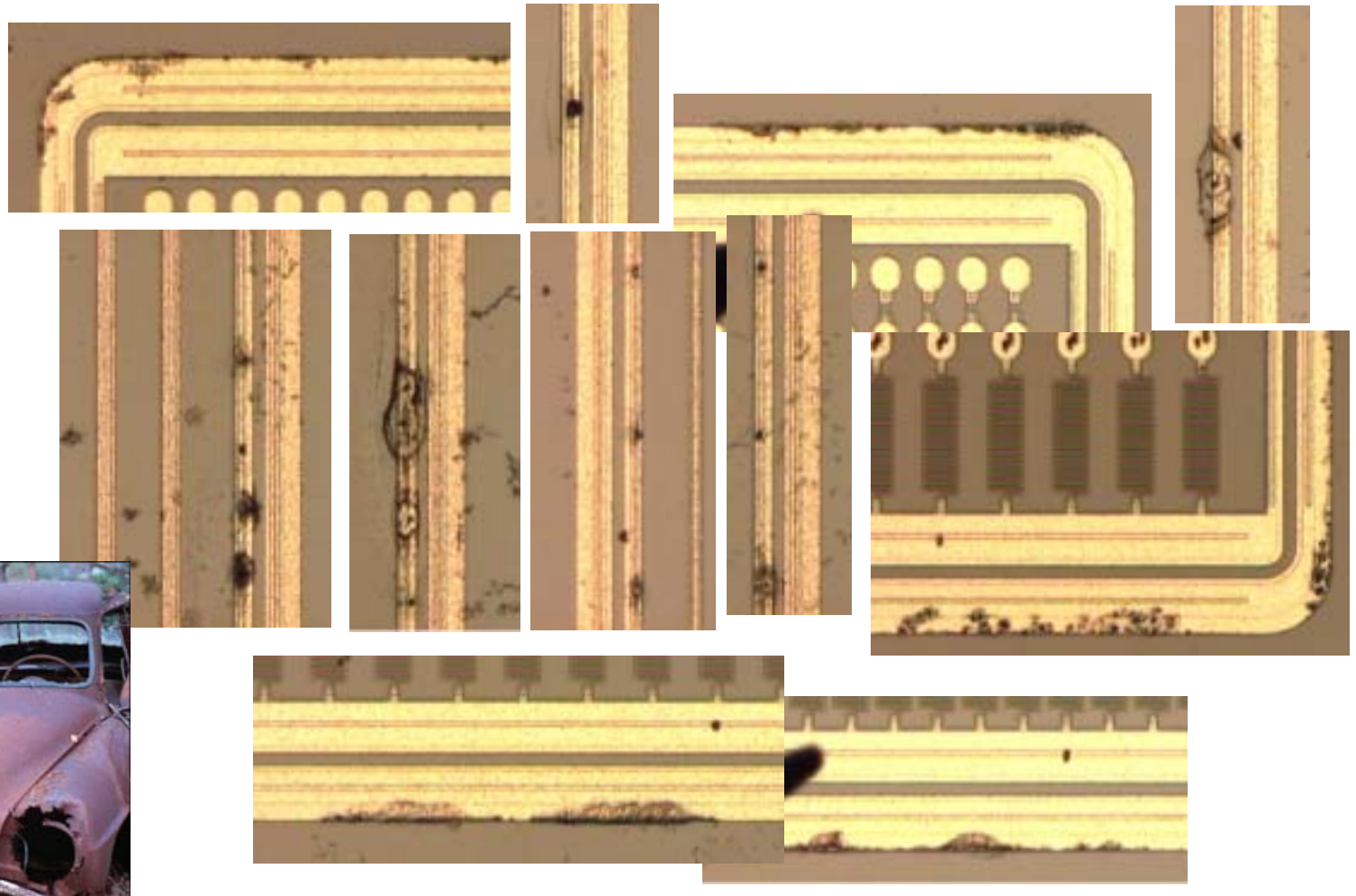
Corrosion on Silicon Sensors

A „How to Eat up Your Detector at the Very End!“

Günther Beuchle, Jean-Charles Fontaine, Martin Frey,
Alexander Furgeri, Frank Hartmann, Manfred Krammer

The most terrible pictures

Stains & Dots: strange colors on our precious sensors



The mystery solved, …

➔ Stains & dots need voltage, time, humidity

- Yes, we all test under bias voltage!
- The company tests only 4 min! ➔ no stains & dots
- Karlsruhe & Vienna test with low humidity
- Strasbourg long term tests sensors from everywhere

BUT, what is it?

And is it dangerous?

この話題に関して興味のある方は、

http://www-conf.kek.jp/vertex2005

Wednesday 09 November 2005

Short Talks and FE Electronics
(09:00->11:50)

Chair: David Christian (FNAL)

Room: Lakeside Hotel--Kaede

Corrosion of Silicon Sensors (20')

Frank Hartmann
(IEKP Karlsruhe, CERN)

を参照してください。

III. Kapton Technology

- **ATLAS, CMS, GLAST all had problems with Kapton**
- **High density (70mm) Al pitch adaptors for PHENIX**
- **Fine pitch (100mm) tab-bonding on ALICE SSD**
- **and ‥‥**

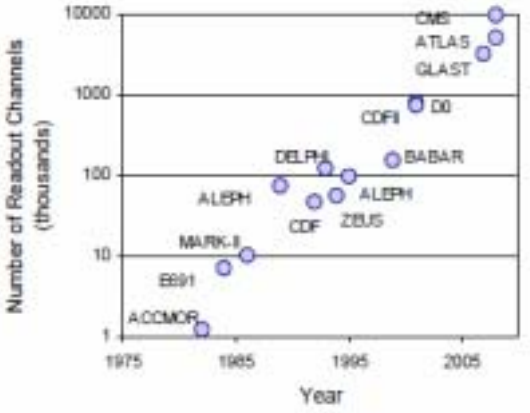
VERTEX2005 @ *Lakeside Hotel, Chuzenji Lake, Nikko*

自分の仕事と関係ない・・・と思っているところに、
今直面している問題解決や、新しい種がたくさん
あることを改めて実感したexcitingな5日間でした。

Worm (RAL) によれば、

What is the next "Big Thing" for vertexing?

- The tracking challenges of reconstructing b/c in high-speed, modern detectors have been met by silicon.
  - Is there room for improvement?
  - What is the next challenge?

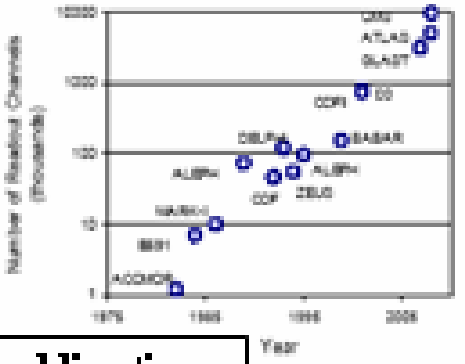


- Bigger?
  - Industrialization of silicon modules made CMS, ATLAS possible
  - More standardisation and simplification needed for any next step
- Better!
  - New technologies(?)
  - Better/thinner detector means charge identification possible
  - Excellent precision in rφ and z; can reconstruct neutrinos in semileptonics

Better detectors needed:
Lower mass, better precision → better understanding of the physics

Steve Worm – RAL/LCFI November 10, 2005 2

Silicon system evolution – Physicist Moores Laws



- *Moores law is often quoted in microelectronics to indicate an exponential change. Compare the situation in 1992 and 2005. Typical values (not the extremes).*

	≤ 1992	2005	Factor	Doubling time
ASIC feature size	5 μm≤5μm	0.25μm≤0.25μm	400	1.5y
Sensor area	0.5 m^2	100 m^2	200	1.7y
Sensor cost/cm2			0.1	4y
Strip channels	10^6	10^7	100	2y
CCD channels	~ 10^8	10^8 - 10^9		-
FE speed	μsec	10 nsec	100	2y
Power/ch	mW	mW	1	compensation

- Cannot extrapolate – hit physical (& financial limits)

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Worm (RAL) によれば、
今や “*bigger*よりも*better detectors*” が必要である！

ということは、量より質・・・ならば我々にもチャンスがある！？・・・may be

三人寄れば文殊の知恵！互いのcommunicationを密にして
MPGD研究会等を盛り上げていって独創性を高めていき、

VERTEX2006 には・・・

是非、日本からも報告を沢山出しましょう！