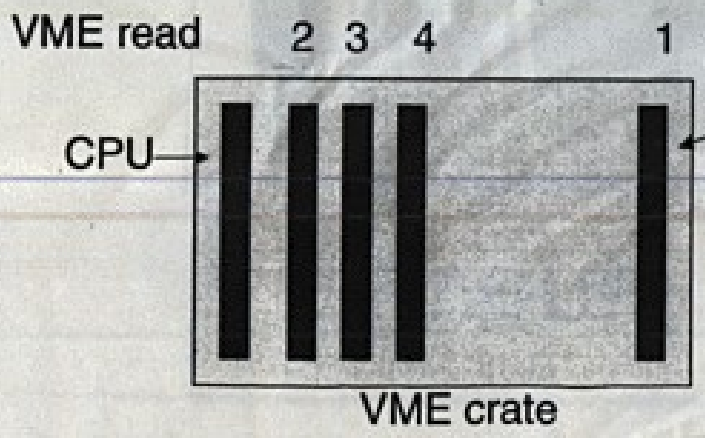
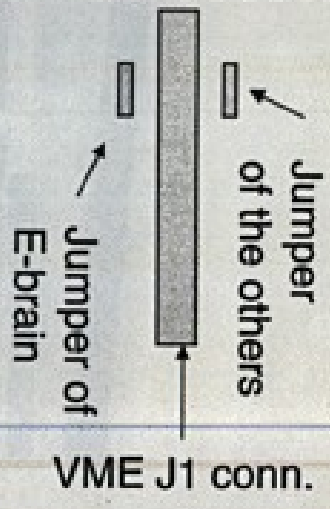
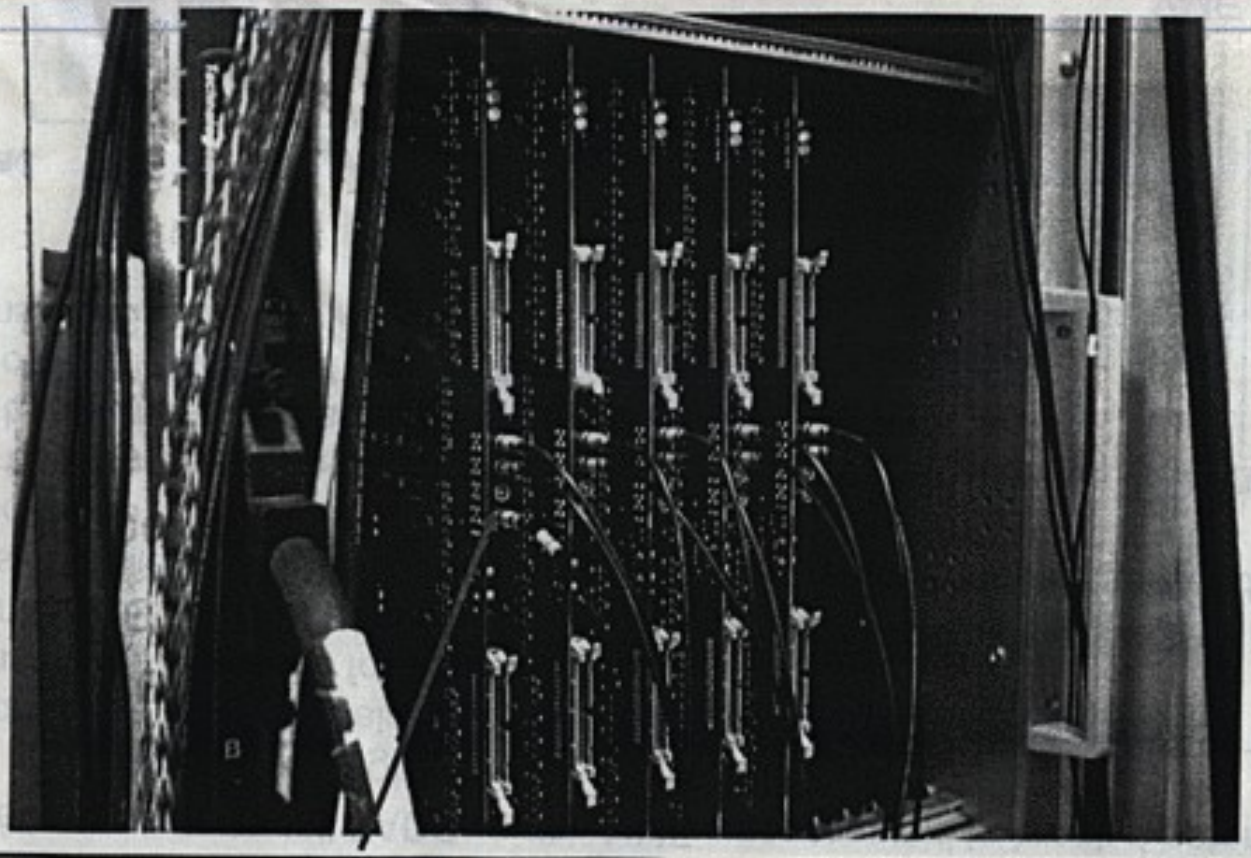
- There is a rule to install FADCs in the VME crate to avoid to break a potentio meter,
  Install from right, remove from left.
- Jumper PINs for IACK belongs to left connector of the 9U crate made by Taiwan and Dennsann but opposite for that by e-brain.
- Download of CPLD is unsuccessful if you use 9~13 modules with a CPU in a crate. The slot beside the CPU is the most problematic, some modules succeed donwload but some do not.
- One board must be on the most right side in a crate. And it sends IRQ and BUSY. This board must be read at first in the collector program.
- The order of VME read makes trouble of mod# & suppr-level inconsistent.



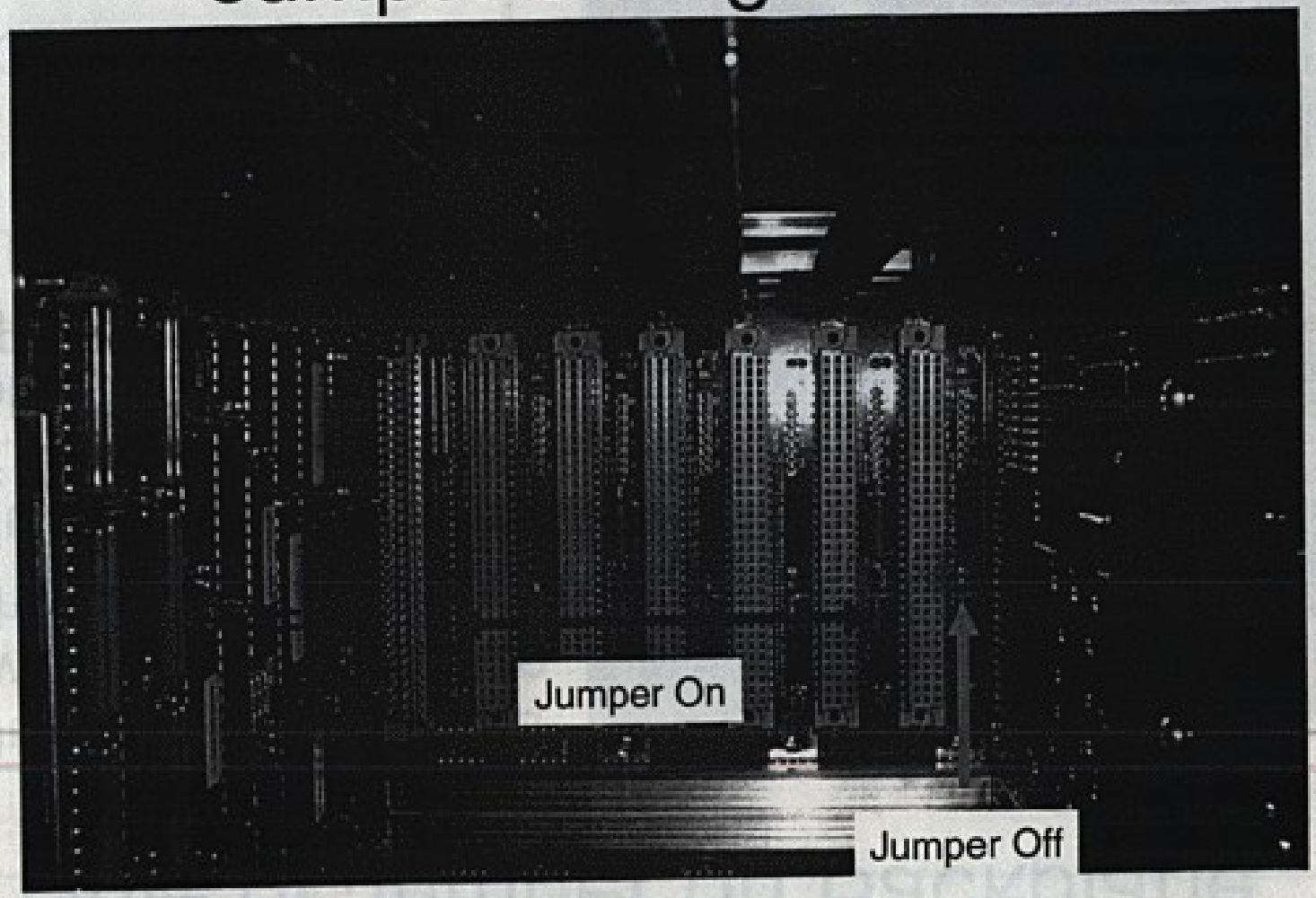


Overall Configuration



1. Only one module per crate sends IRQ.
2. The "reset" and "trigger-enable" of the module, whose BUSY is connected to trigger veto, in DAQ should be the last one in the DAQ.

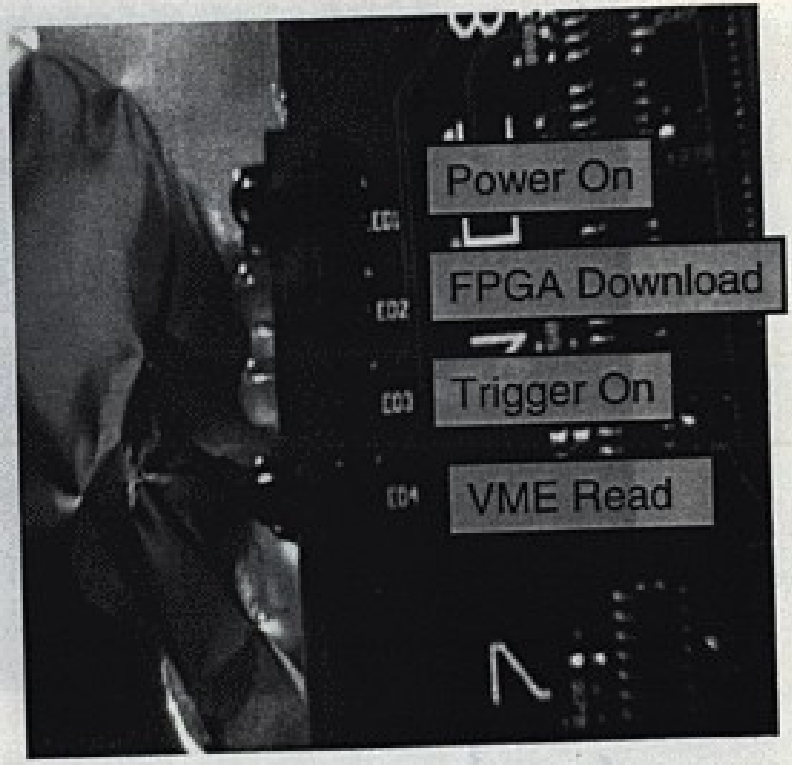
Zoom-In View of Jumper Configuration



Rule of Jumper on Backplane

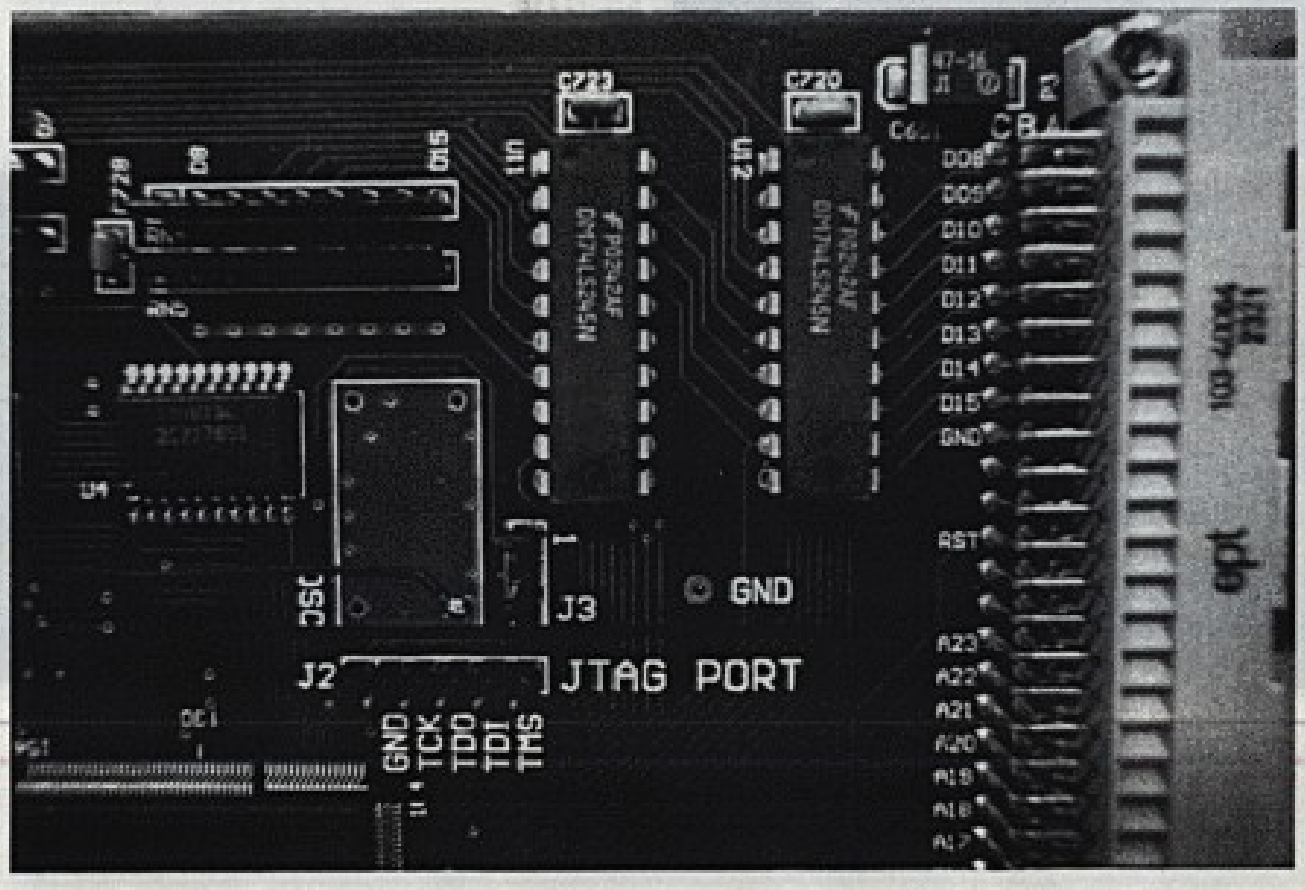
- Jumper is associated with the connector on the near right side.
- Jumper should be on if the connector is not plugged with FADC. (Red box)
- Jumper should be off if the connector is plugged with FADC. (Green box)

Lemo Connector & LED Light

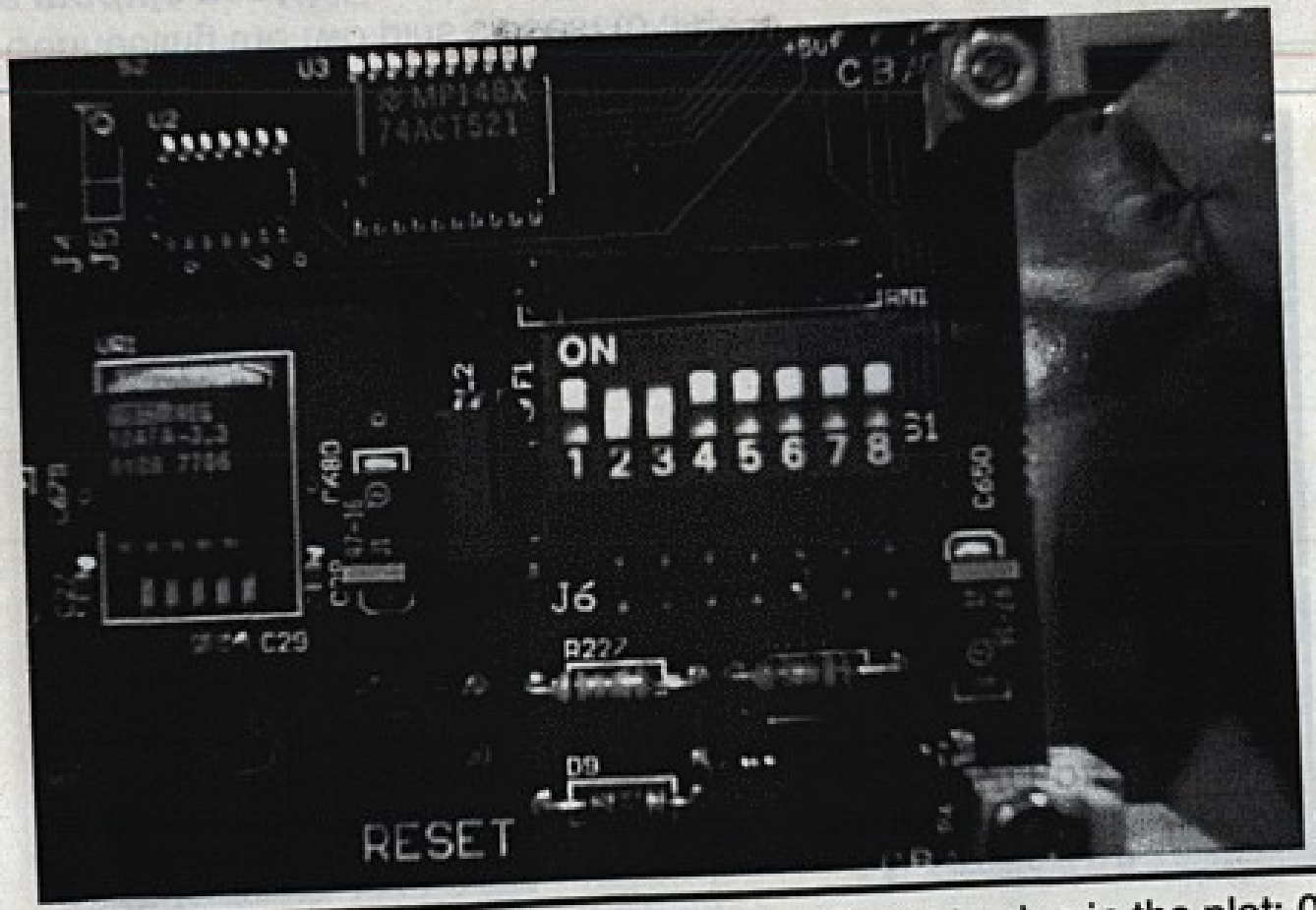


MADE IN JAPAN

Xilinx JTAG Download (J2)

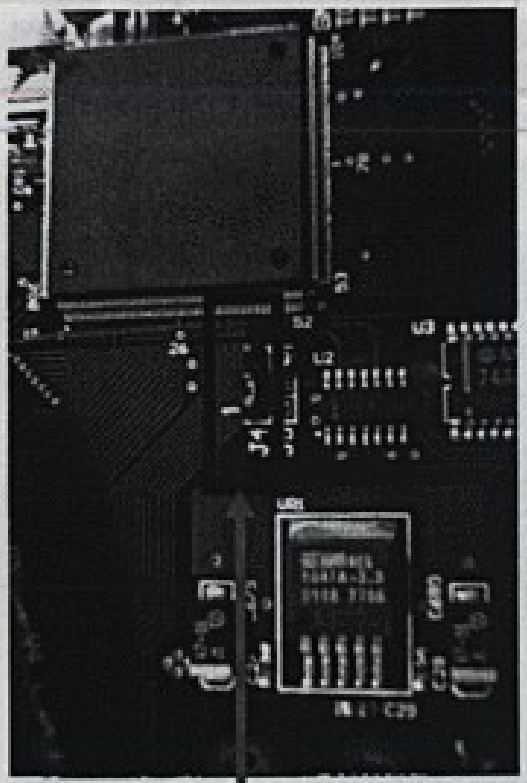


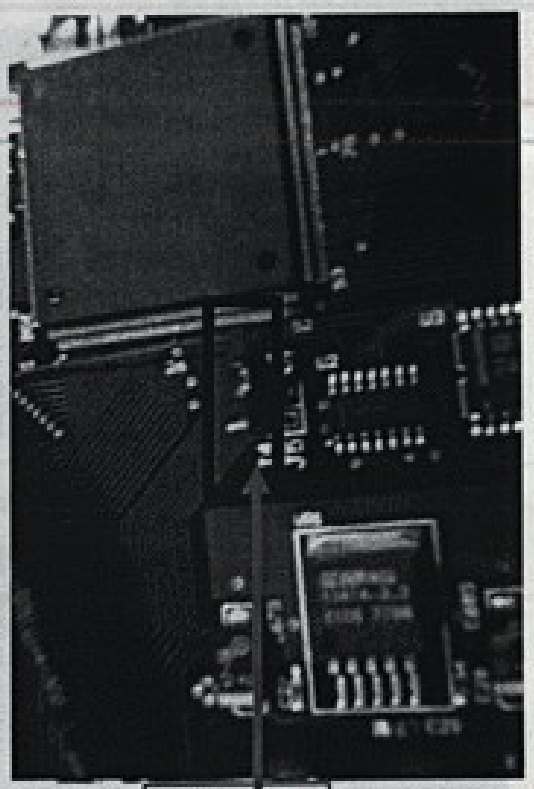
VME Base Address Switch (S1)



Binary setting. Lowest Bit: 1. Up=off; Down=on. Current value in the plot: 0x060000.

IRQ Jumper (J4)

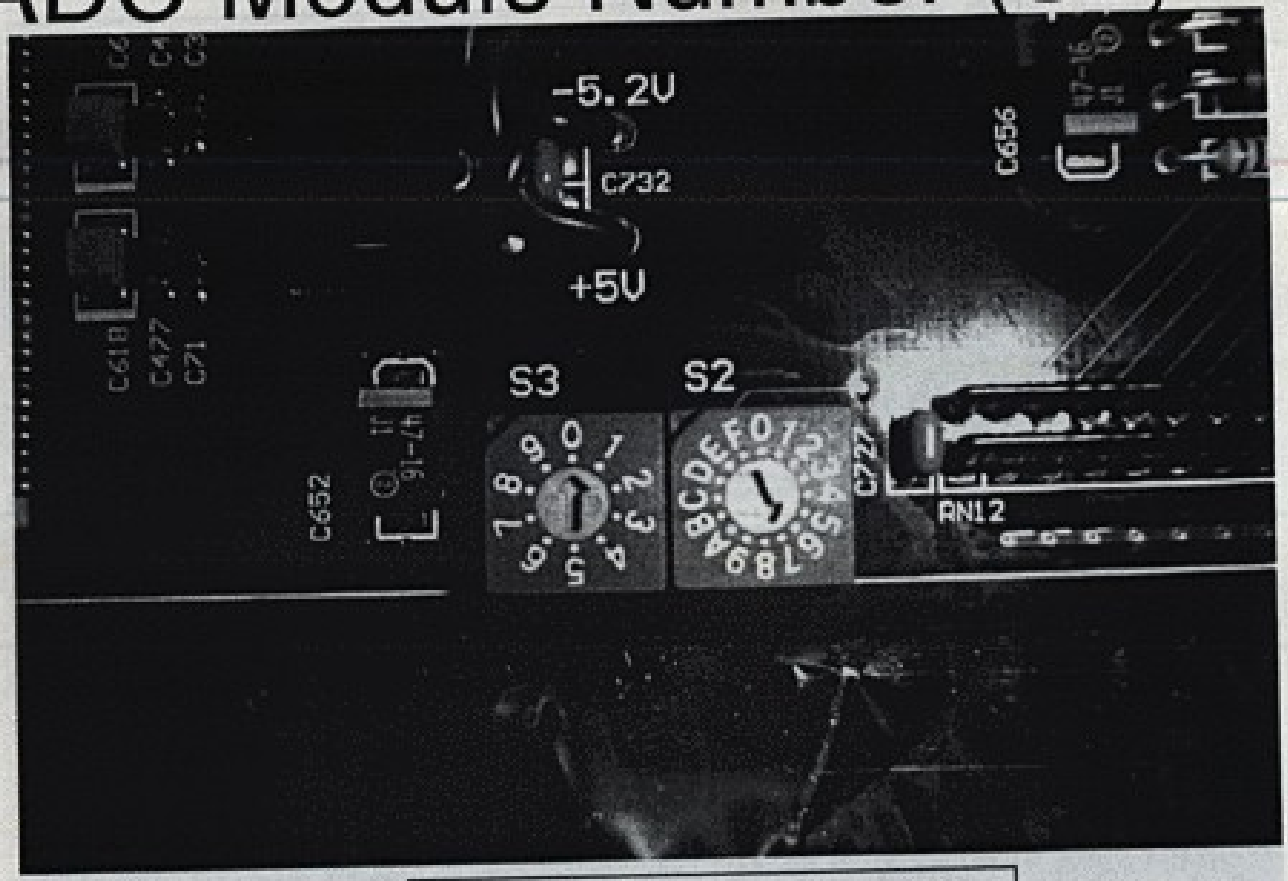




IRQ-off

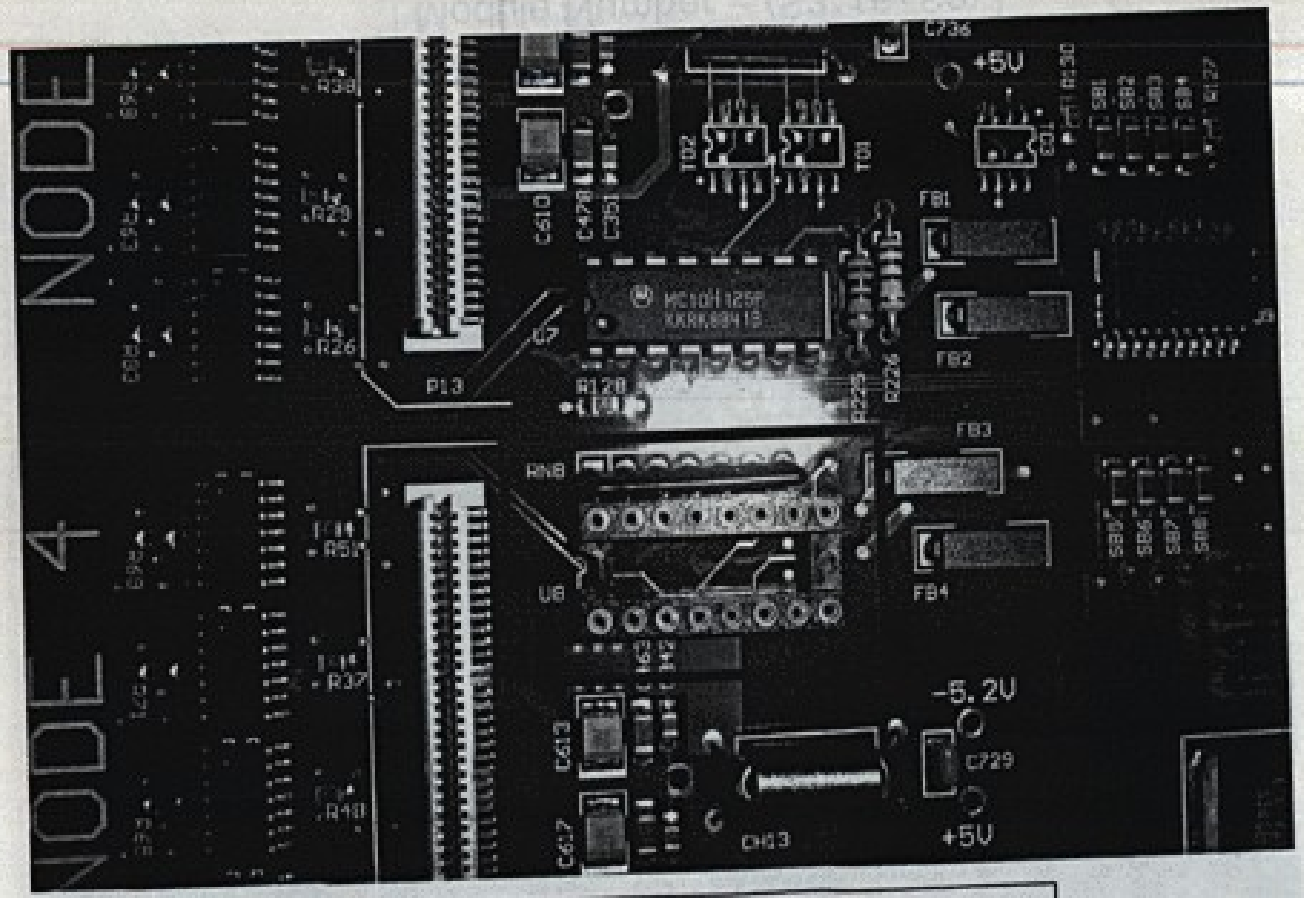
IRQ-on: Connecting the two pins closest to J4.
Only one module per VME crate, sitting closest to the VME repeater.
The jumper on VME backplane must be on between IRQ module and VME repeater.

FADC Module Number (S2, S3)



Module Number in Header2:
Module Number = (S3*16+S2)
Module Number above = 7

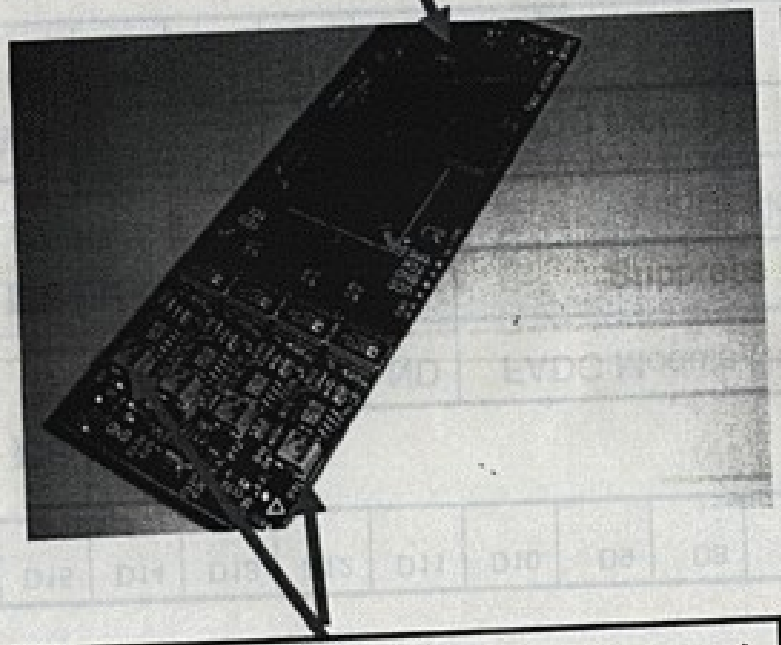
IC for BUSY Signal (U8)



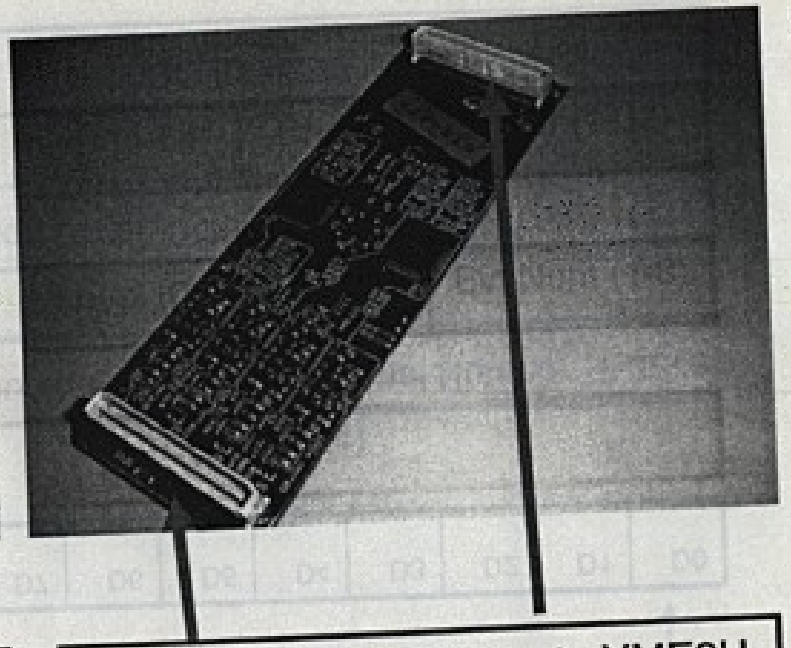
IC: MC10124-U8, dip16. Half-circle mark on the left.

4-channel FADC card

Screw hole for fastening and ground.



Potential-Meter for pedestal adjustment.



Connectors for fastening to VME9U.

CS: Checksum bit

ND: Not defined.

Data Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Header 1

CS	0	0	ND	ND	FADC Module Number (1-64)	Channel Number (1-32)

Header 2

CS	0	0	ND	ND	Suppression Level (0-255)	Evt Num (1-8)

ADC

CS	0	1	H1	H2	H3	ADC (0-1024)

Time

CS	1	0	H1	H2	H3	Time (0-1024)

Trailer

CS	1	1	H1	H2	H3	Number of ADC data bins (0-1024)

Data Format

- **Header1,2:**

  D14, D13 : identifier

  D15 = D0 (XOR) D1 (XOR) D2 ..... (XOR) D11 (XOR) D12 ,

- **ADC, TDC, TRAILER:**

  D14, D13 : identifier

  CS=D15 = D0 (XOR) D1 (XOR) D2 ..... (XOR) D10

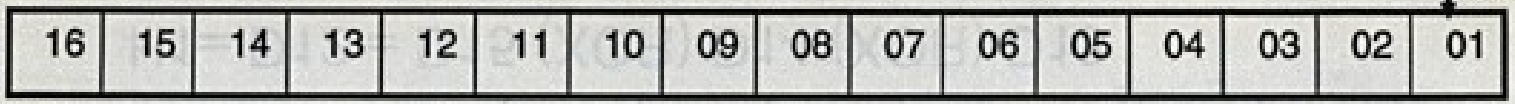
  H1= D12 = D15 (XOR) D14 (XOR) D13

  H2= D11 = D15 (XOR) D14 (XOR) D0

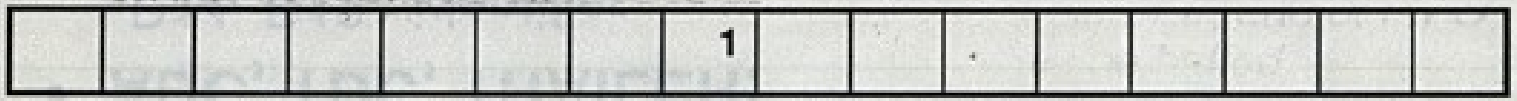
  H3= D10 = D15 (XOR) D13 (XOR) D0

CSR Format

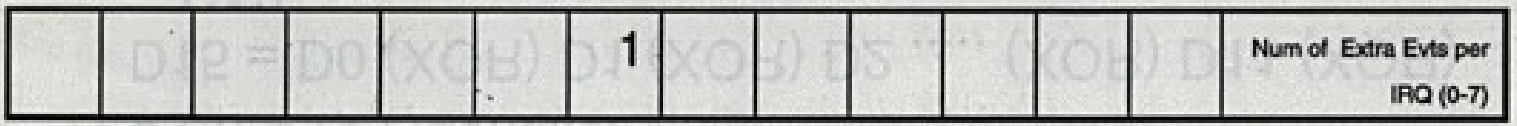
CSR address: 0x0i0000, i = the value set in S1.



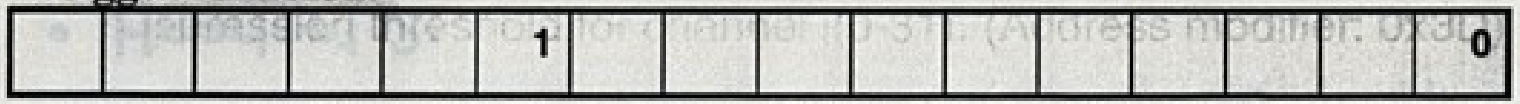
Reset: clear counters, FIFO, BUSY.



Number of Events stored in FIFO before issuing IRQ



Trigger Disabled:



Trigger Enabled: change of event number/IRQ is not allowed.

FADC VME Action List for Module with VME address 0x0i000 (A24/D16)

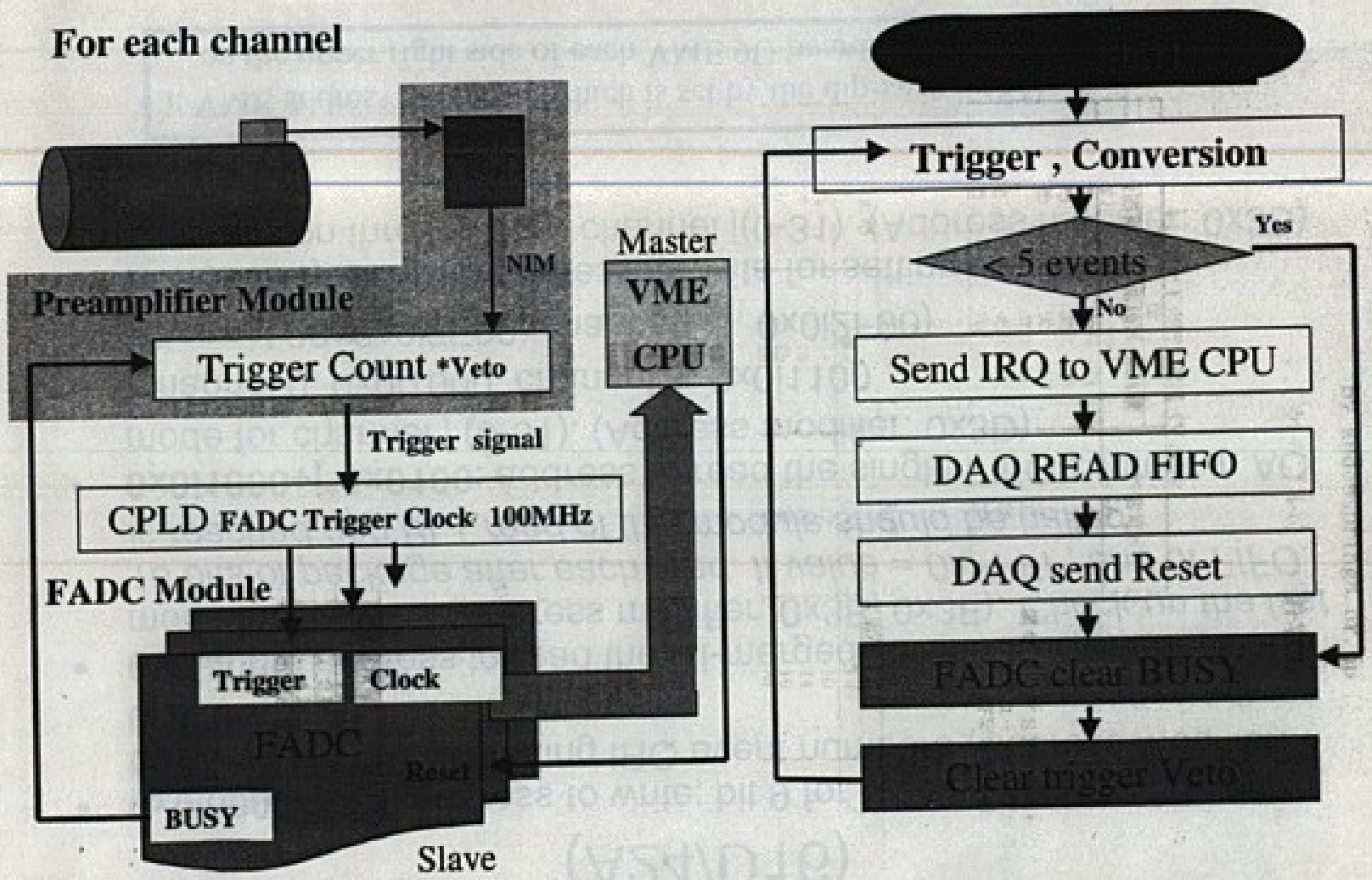
- **0x0i0000**: CSR address to write; bit 9 for resetting FIFO and clear busy, bit 1-4, 10 for setting IRQ event numbers (Address modifier: 0x3D).
- **0x0i4000**: address to read the all-merged 32 FIFOs' content in BLT mode for FADC i. (Address modifier: 0x3B, 0x3F). *Check up the last 16 bits of package after each read. If value = 0xFFFF, end of FIFO is reached and BLT read of this module should be halted.*
- **0x0i1000+j*0x0100**: address to read the single FIFO content in AO mode for channel j (0-31). (Address modifier: 0x3D)

  (channel 0, 0x0i1000, channel 1, 0x0i1100 ,....

  channel 30, 0x0i2E00, channel 31, 0x0i2F00)
- **0x0i1000+j*0x0100**: address to write for setting the zero-suppression threshold for channel j(0-31). (Address modifier: 0x3D)

i: VME address definition which is set by the dip-switch (S1) on the upper right side of each VME 9U board, starting from 1.

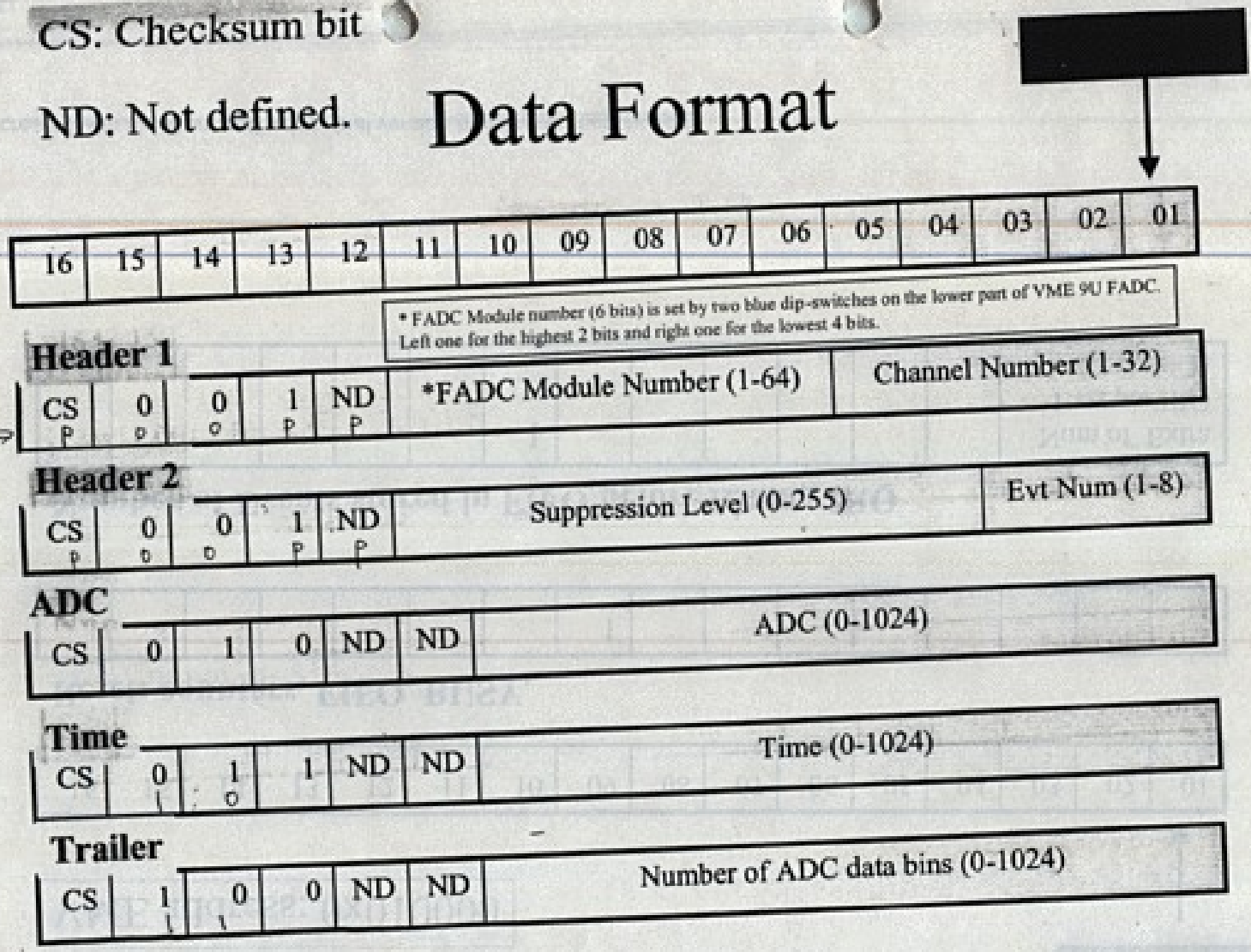
The Control Flow of FADC



CS: Checksum bit

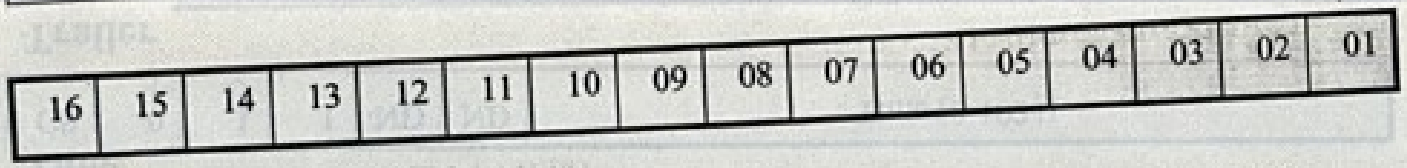
ND: Not defined.

Data Format

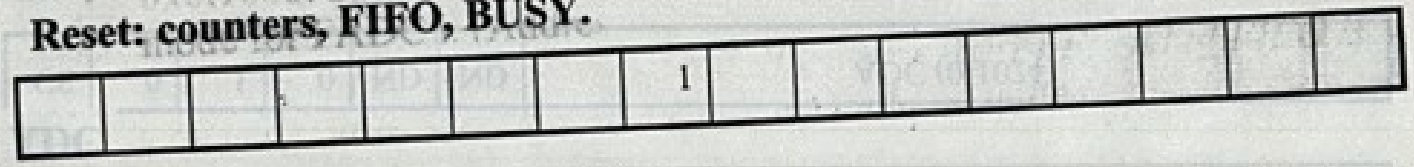


CSR Format

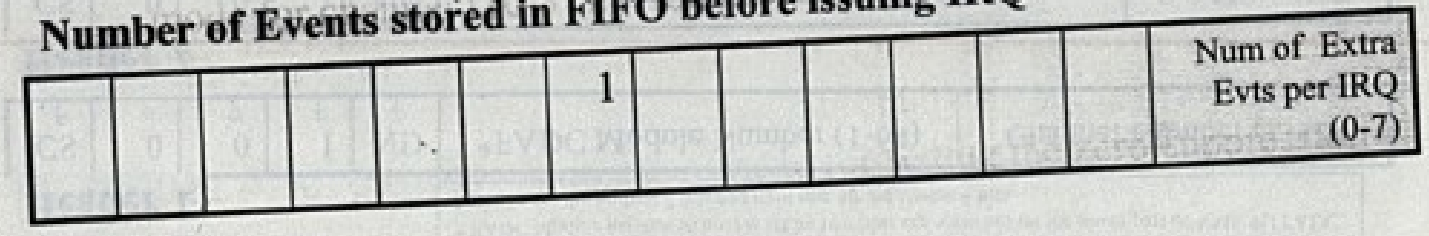
VME address: 0x010000



Reset: counters, FIFO, BUSY.



Number of Events stored in FIFO before issuing IRQ



FADC VME Action List (A24/D16)

- **0x0i0000**: CSR address to write; bit 9 for resetting FIFO and clear busy, bit 1-4, 10 for setting IRQ event numbers (Address modifier: 0x3D).
- **0x0i1000**: address to read the all-merged 32 FIFOs' content in BLT mode for FADC i. (Address modifier: 0x3B, 0x3F). *Check up the last 16 bits of package after each read. If value = 0xFFFF, end of FIFO is reached and BLT read of this module should be halted.*
- **0x0i1000+j*0x0100**: address to read the single FIFO content in AO mode for channel j (0-31). (Address modifier: 0x3D)

  (channel 0, 0x0i1000, channel 1, 0x0i1100 ,....

  channel 30, 0x0i2E00, channel 31, 0x0i2F00)
- **0x0i1000+j*0x0100**: address to write for setting the zero-suppression threshold for channel j(0-31). (Address modifier: 0x3D)

i: module number for VME address definition which is set by the dip-switch on the upper right side of each VME 9U board.

The Control Flow of FADC